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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20j15a-au

- – Up to five 16-bit Timer/Counters (TC), configurable as either:
  - • One 16-bit TC with two compare/capture channels
  - • One 8-bit TC with two compare/capture channels
  - • One 32-bit TC with two compare/capture channels, by using two TCs
- – 32-bit Real Time Counter (RTC) with clock/calendar function
- – Watchdog Timer (WDT)
- – CRC-32 generator
- – Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
  - • USART with full-duplex and single-wire half-duplex configuration
  - • Inter-Integrated Circuit (I^2C) up to 400kHz
  - • Serial Peripheral Interface (SPI)
- – One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
  - • Differential and single-ended input
  - • 1/2x to 16x programmable gain stage
  - • Automatic offset and gain error compensation
  - • Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- – 10-bit, 350ksps Digital-to-Analog Converter (DAC)
- – Two Analog Comparators (AC) with window compare function
- – Peripheral Touch Controller (PTC)
  - • 256-Channel capacitive touch and proximity sensing
- • I/O
  - – Up to 52 programmable I/O pins
- • Packages
  - – 64-pin TQFP, QFN
  - – 64-ball UFBGA
  - – 48-pin TQFP, QFN
  - – 45-ball WLCSP
  - – 32-pin TQFP, QFN
- • Operating Voltage
  - – 1.62V – 3.63V
- • Power Consumption
  - – Down to 70µA/MHz in active mode
  - – Down to 8µA running the Peripheral Touch Controller

2. Configuration Summary

	SAM D20J	SAM D20G	SAM D20E
Pins	64	48	32
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32KB	256/128/64/32KB	256/128/64/32KB
SRAM	32/16/8/4/2KB	32/16/8/4/2KB	32/16/8/4/2KB
Timer Counter (TC) instances	8	6	6
Waveform output channels per TC instance	2	2	2
Serial Communication Interface (SERCOM) instances	6	6	4
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Maximum CPU frequency	48MHz		
Packages	QFN TQFP UFBGA	QFN TQFP WLCSP	QFN TQFP
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M)		
Event System channels	8	8	8
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20E14A	0x0E	0x1000130E
Reserved	0x0F	
SAMD20G18U	0x10	0x10001310
SAMD20G17U	0x11	0x10001311
Reserved	0x12 - 0xFF	

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4.   Block Diagram

Note: 1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to *Peripherals Configuration Summary* for details.
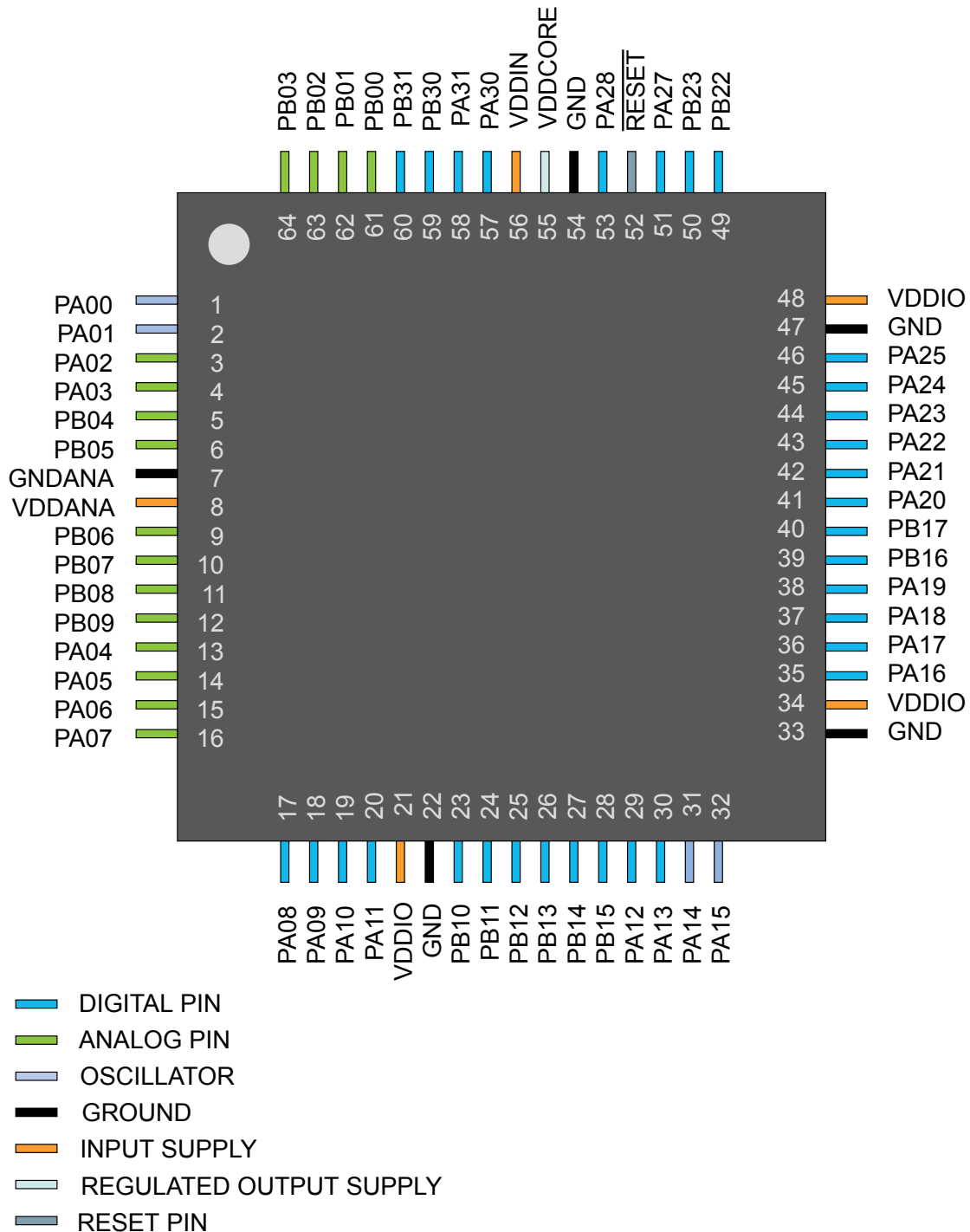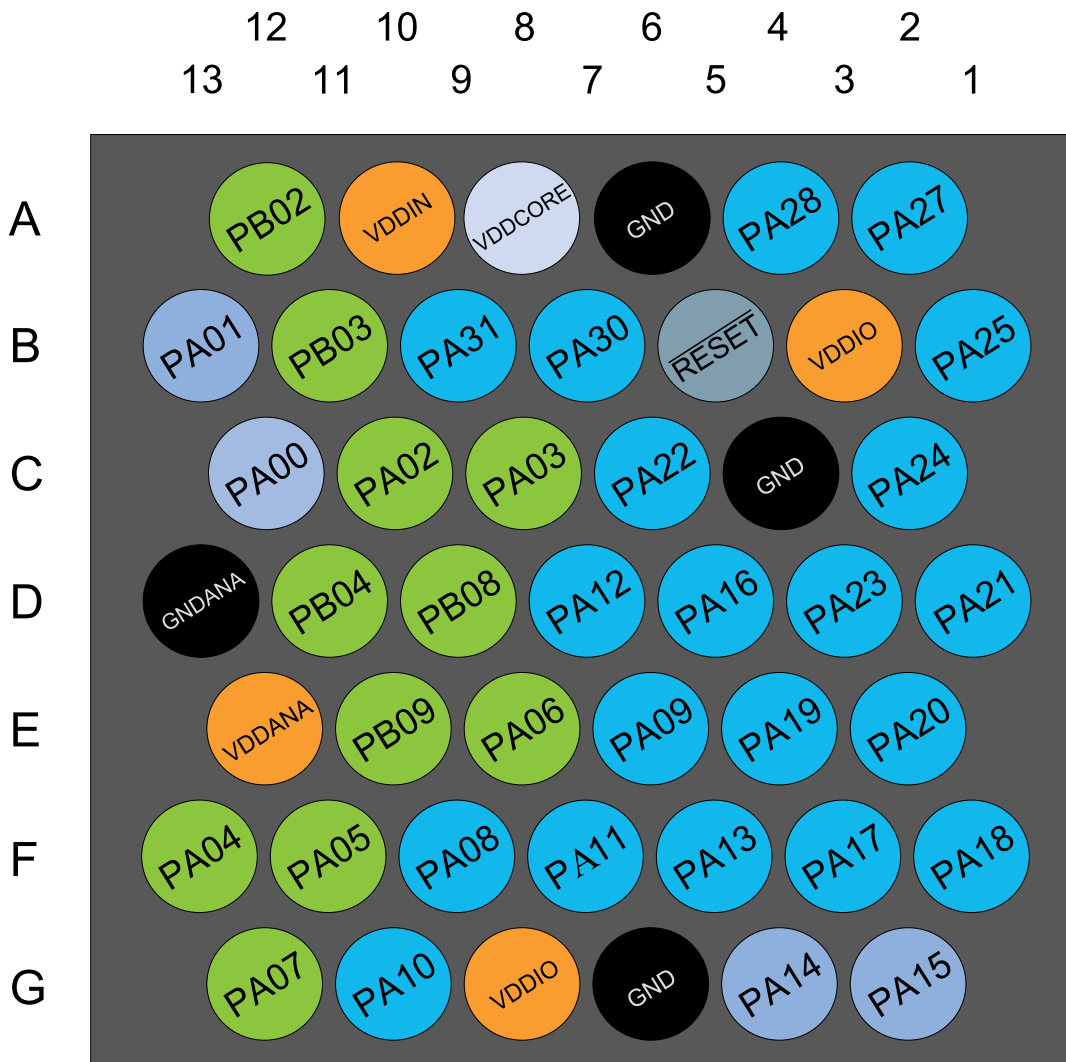
5. Pinout

5.1. SAM D20J

5.1.1. QFN64 / TQFP64

- ▬ DIGITAL PIN
- ▬ ANALOG PIN
- ▬ OSCILLATOR
- ▬ GROUND
- ▬ INPUT SUPPLY
- ▬ REGULATED OUTPUT SUPPLY
- ▬ RESET PIN

5.2.2. WLCSP45

DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

7. Processor And Architecture

7.1. Cortex M0+ Processor

The SAM D20 implements the ARM® Cortex®-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to http://www.arm.com.

7.1.1. Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration

Features	Configurable option	Device configuration
Interrupts	External interrupts 0-32	28
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent[1]
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note:

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

7.1.2. Cortex-M0+ Peripherals

- System Control Space (SCS)
    - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Timer (SysTick)

- – The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
  - – External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Control Block (SCB)
  - – The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (www.arm.com).
- Micro Trace Buffer (MTB)
  - – The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

7.1.3. Cortex-M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000 (see also Product Mapping)	Micro Trace Buffer (MTB)

7.1.4. I/O Interface

7.1.4.1. Overview
Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

7.1.4.2. Description
Direct access to PORT registers.

7.2. Nested Vector Interrupt Controller

7.2.1. Overview
The Nested Vectored Interrupt Controller (NVIC) in the SAM D20 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (www.arm.com).

7.2.2. Interrupt Line Mapping
Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear

(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager	0
SYSCTRL – System Control	1
WDT – Watchdog Timer	2
RTC – Real Time Counter	3
EIC – External Interrupt Controller	4
NVMCTRL – Non-Volatile Memory Controller	5
EVSYS – Event System	6
SERCOM0 – Serial Communication Interface 0	7
SERCOM1 – Serial Communication Interface 1	8
SERCOM2 – Serial Communication Interface 2	9
SERCOM3 – Serial Communication Interface 3	10
SERCOM4 – Serial Communication Interface 4	11
SERCOM5 – Serial Communication Interface 5	12
TC0 – Timer Counter 0	13
TC1 – Timer Counter 1	14
TC2 – Timer Counter 2	15
TC3 – Timer Counter 3	16
TC4 – Timer Counter 4	17
TC5 – Timer Counter 5	18
TC6 – Timer Counter 6	19
TC7 – Timer Counter 7	20
ADC – Analog-to-Digital Converter	21
AC – Analog Comparator	22

Write-protect registers allow the user to disable a selected peripheral's write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral n is write-protected and a write to one in WPSET[n] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

7.7.   Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

Related Links
Product Mapping on page 19

7.7.1.   PAC0 Register Description

7.7.1.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 6 – EIC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.2.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000002
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		MTB			PORT	NVMCTRL	DSU	
Access		R/W			R/W	R/W	R/W	
Reset		0			0	0	1	

Bit 6 – MTB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.3.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 15,14,13,12,11,10,9,8 – TCx

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 7,6,5,4,3,2 – SERCOMx

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 15,14,13,12,11,10,9,8 – TCx
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 7,6,5,4,3,2 – SERCOMx
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E8

8.2.4. 48 pin TQFP

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

See detail

0° to 7°

11 - 13 °

0.102 max.
LEAD COPLANARITY

DETAIL VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e	0.50 BSC			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.
Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

Package Drawing Contact:
packagedrawings@atmel.com

TITLE	GPC	DRAWING NO.	REV.
MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	ALV	MC	E

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 45-ball WLCSP

DRAWINGS NOT SCALED

COMMON DIMENSIONS (Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A2	PA27	-1	1.039
A4	PA28	-0.6	1.039
A6	GNDIO05	-0.2	1.039
A8	VDDCORE	0.2	1.039
A10	VDDIN	0.6	1.039
A12	PB02	1	1.039
B1	PA25	-1.2	0.693
B3	VDDIO04	-0.8	0.693
B5	RESET_N	-0.4	0.693
B7	PA30	0	0.693
B9	PA31	0.4	0.693
B11	PB03	0.8	0.693
B13	PA01	1.2	0.693
C2	PA24	-1	0.346
C4	GNDIO04	-0.6	0.346
C6	PA22	-0.2	0.346
C8	PA03	0.2	0.346
C10	PA02	0.6	0.346
C12	PA00	1	0.346
D1	PA21	-1.2	0.000
D3	PA23	-0.8	0.000
D5	PA16	-0.4	0.000
D7	PA12	0	0.000

BALL	SIGNAL	X COORD	Y COORD
D9	PB08	0.4	0.000
D11	PB04	0.8	0.000
D13	GNDANA	1.2	0.000
E2	PA20	-1	-0.346
E4	PA19	-0.6	-0.346
E6	PA09	-0.2	-0.346
E8	PA06	0.2	-0.346
E10	PB09	0.6	-0.346
E12	VDDANA	1	-0.346
F1	PA18	-1.2	-0.693
F3	PA17	-0.8	-0.693
F5	PA13	-0.4	-0.693
F7	PA11	0	-0.693
F9	PA08	0.4	-0.693
F11	PA05	0.8	-0.693
F13	PA04	1.2	-0.693
G2	PA15	-1	-1.039
G4	PA14	-0.6	-1.039
G6	GNDIO02	-0.2	-1.039
G8	VDDIO02	0.2	-1.039
G10	PA10	0.6	-1.039
G12	PA07	1	-1.039

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

07/07/2014

Package Drawing Contact: packagedrawings@atmel.com

TITLE: VH, 45 ball (13x7 Array), 0.4mm pitch 2.944 x 2.699 x 0.483mm, WLCSP

GPC: GKG

DRAWING NO.: VH

REV.: B

TOP VIEW — PIN A1 CORNER — 2.699+/-0.03 — 2.944+/-0.03 — 0.03 (4X)

BOTTOM VIEW — A1 CORNER — 2.079 — 2.400 — 0.400 — 0.20 — b=Ø 0.260+/-0.030 (45X)

SIDE VIEW — 0.075 C — 0.483 max — 0.20 +/- 0.03 — SEATING PLANE — Backside Coating : 0.04mm — 0.203 +/- 0.025

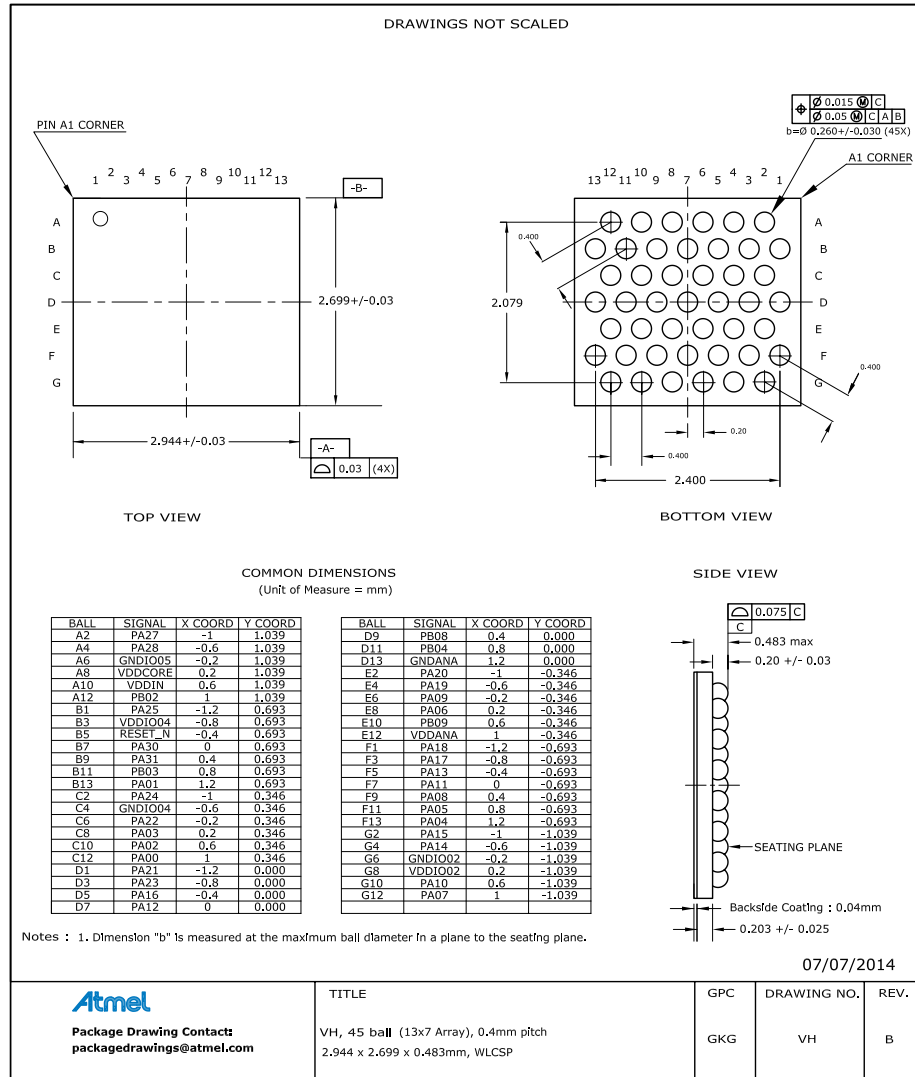**Table 8-17. Device and Package Maximum Weight**

7.3	mg

Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.2.7. 32 pin TQFP

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

0°~7°

BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.
Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

Package Drawing Contact:
packagedrawings@atmel.com

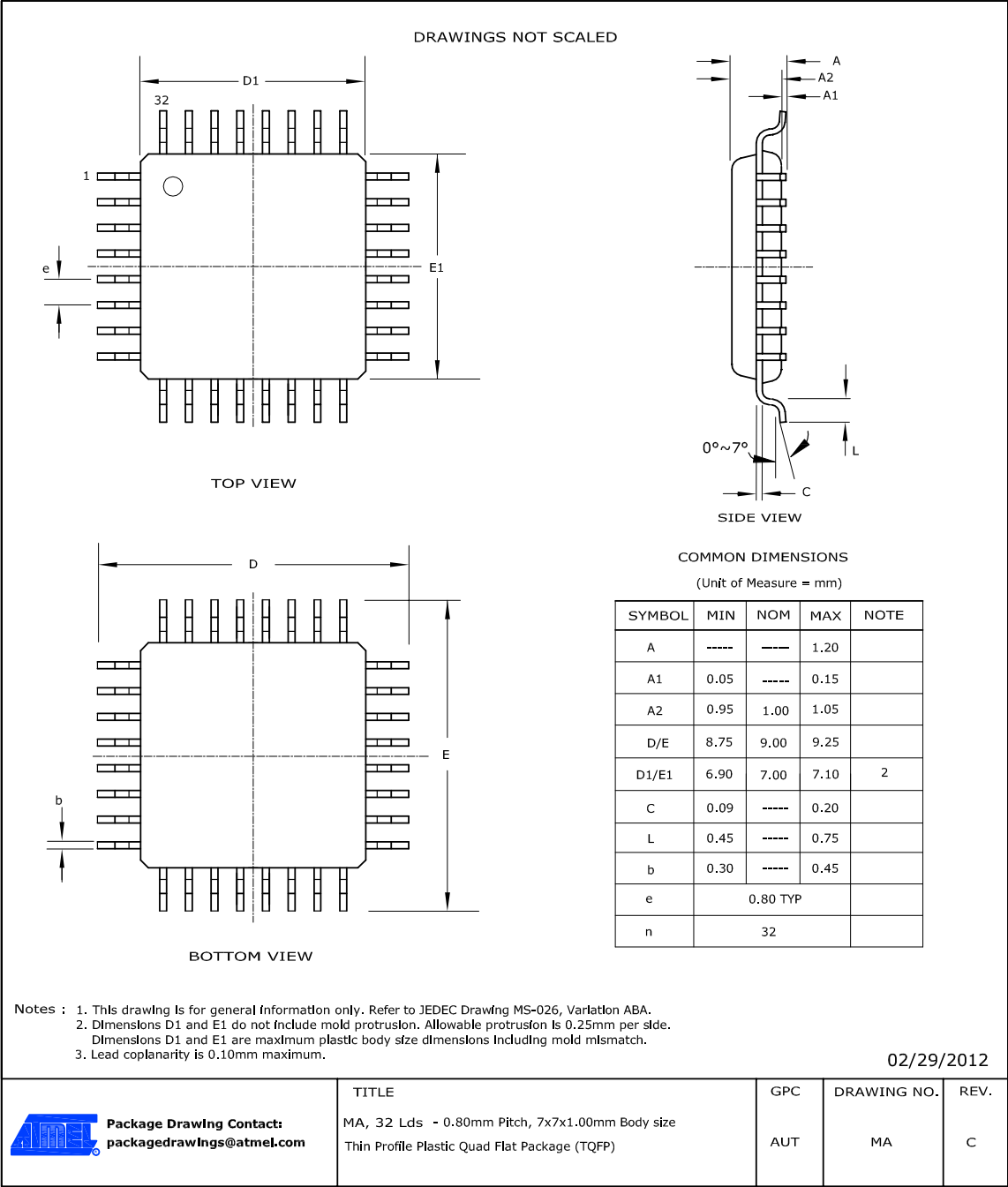| TITLE	GPC	DRAWING NO.	REV.
MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

Table 8-20. Device and Package Maximum Weight

100	mg

Table 8-21. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.3.   Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-29.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.