



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

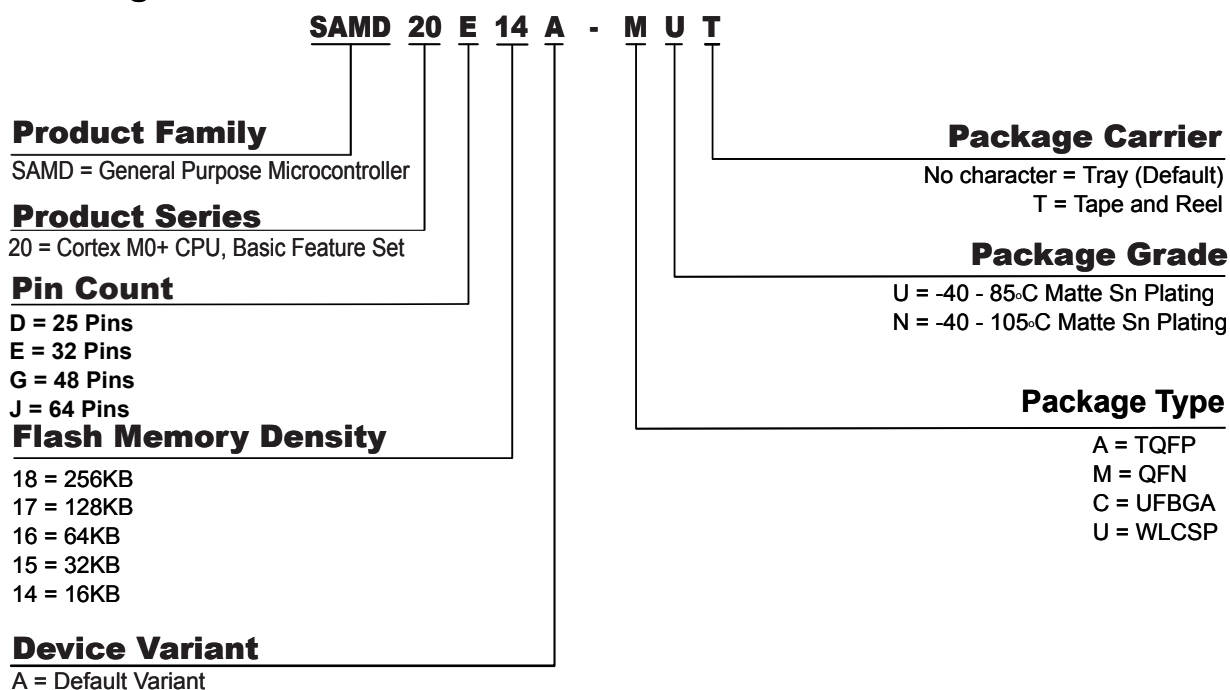
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20j16a-ant

3. Ordering Information



3.1. SAM D20E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E14A-AU	16K	2K	TQFP32	Tray
ATSAMD20E14A-AUT				Tape & Reel
ATSAMD20E14A-AN				Tray
ATSAMD20E14A-ANT				Tape & Reel
ATSAMD20E14A-MU			QFN32	Tray
ATSAMD20E14A-MUT				Tape & Reel
ATSAMD20E14A-MN				Tray
ATSAMD20E14A-MNT				Tape & Reel

3.2. SAM D20G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G14A-AU	16K	2K	TQFP32	Tray
ATSAMD20G14A-AUT				Tape & Reel
ATSAMD20G14A-AN				Tray
ATSAMD20G14A-ANT				Tape & Reel
ATSAMD20G14A-MU			QFN32	Tray
ATSAMD20G14A-MUT				Tape & Reel
ATSAMD20G14A-MN				Tray
ATSAMD20G14A-MNT				Tape & Reel
ATSAMD20G15A-AU	32K	4K	TQFP48	Tray
ATSAMD20G15A-AUT				Tape & Reel
ATSAMD20G15A-AN				Tray
ATSAMD20G15A-ANT				Tape & Reel
ATSAMD20G15A-MU			QFN48	Tray
ATSAMD20G15A-MUT				Tape & Reel
ATSAMD20G15A-MN				Tray
ATSAMD20G15A-MNT				Tape & Reel
ATSAMD20G16A-AU	64K	8K	TQFP48	Tray
ATSAMD20G16A-AUT				Tape & Reel
ATSAMD20G16A-AN				Tray
ATSAMD20G16A-ANT				Tape & Reel
ATSAMD20G16A-MU			QFN48	Tray
ATSAMD20G16A-MUT				Tape & Reel
ATSAMD20G16A-MN				Tray
ATSAMD20G16A-MNT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J15A-AU	32K	4K	TQFP64	Tray
ATSAMD20J15A-AUT				Tape & Reel
ATSAMD20J15A-AN				Tray
ATSAMD20J15A-ANT				Tape & Reel
ATSAMD20J15A-MU			QFN64	Tray
ATSAMD20J15A-MUT				Tape & Reel
ATSAMD20J15A-MN				Tray
ATSAMD20J15A-MNT				Tape & Reel
ATSAMD20J16A-AU	64K	8K	TQFP64	Tray
ATSAMD20J16A-AUT				Tape & Reel
ATSAMD20J16A-AN				Tray
ATSAMD20J16A-ANT				Tape & Reel
ATSAMD20J16A-MU			QFN64	Tray
ATSAMD20J16A-MUT				Tape & Reel
ATSAMD20J16A-MN				Tray
ATSAMD20J16A-MNT				Tape & Reel
ATSAMD20J16A-CU			UFBGA64	Tray
ATSAMD20J16A-CUT				Tape & Reel
ATSAMD20J17A-AU	128K	16K	TQFP64	Tray
ATSAMD20J17A-AUT				Tape & Reel
ATSAMD20J17A-AN				Tray
ATSAMD20J17A-ANT				Tape & Reel
ATSAMD20J17A-MU			QFN64	Tray
ATSAMD20J17A-MUT				Tape & Reel
ATSAMD20J17A-MN				Tray
ATSAMD20J17A-MNT				Tape & Reel
ATSAMD20J17A-CU			UFBGA64	Tray
ATSAMD20J17A-CUT				Tape & Reel

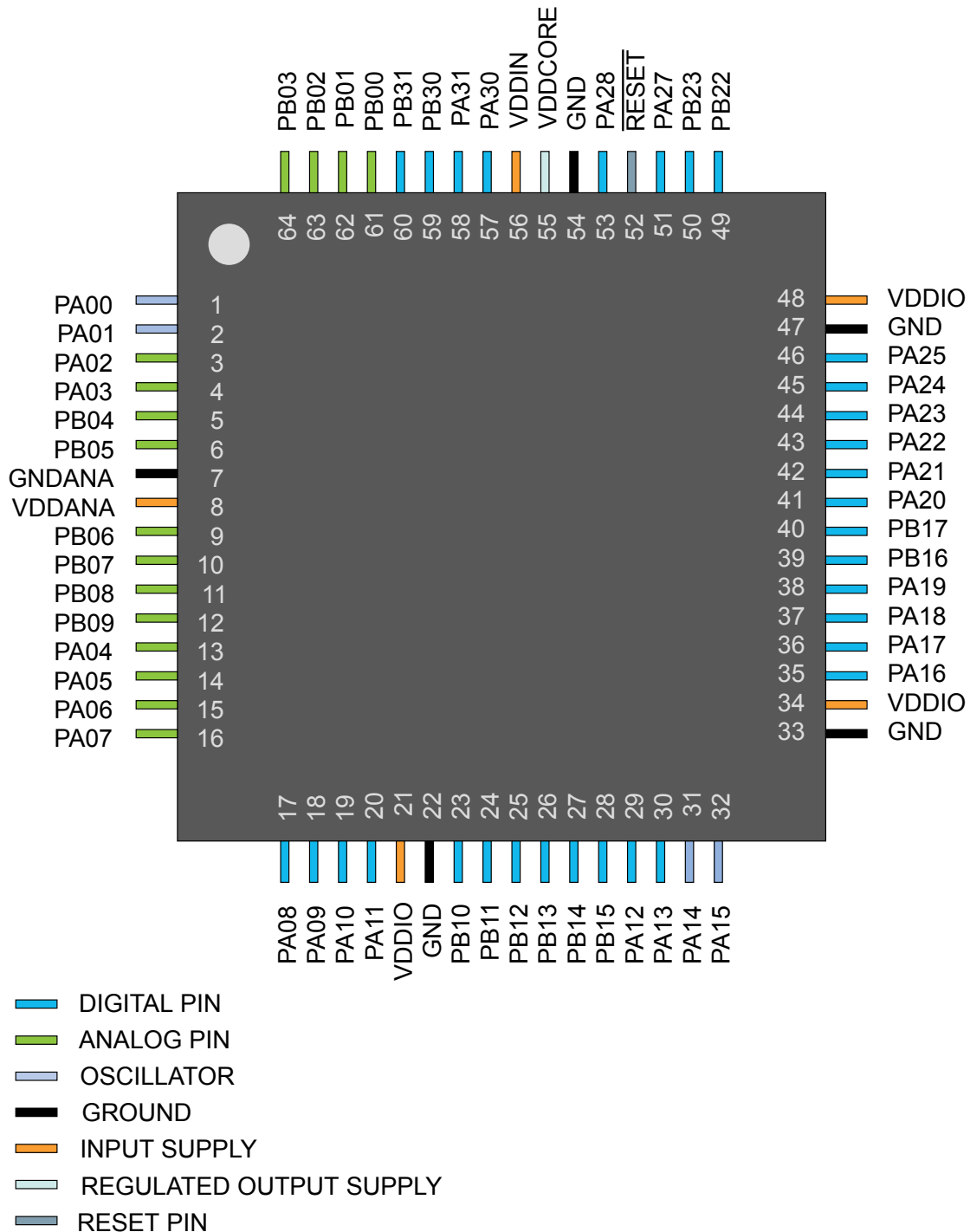
Atmel



5. Pinout

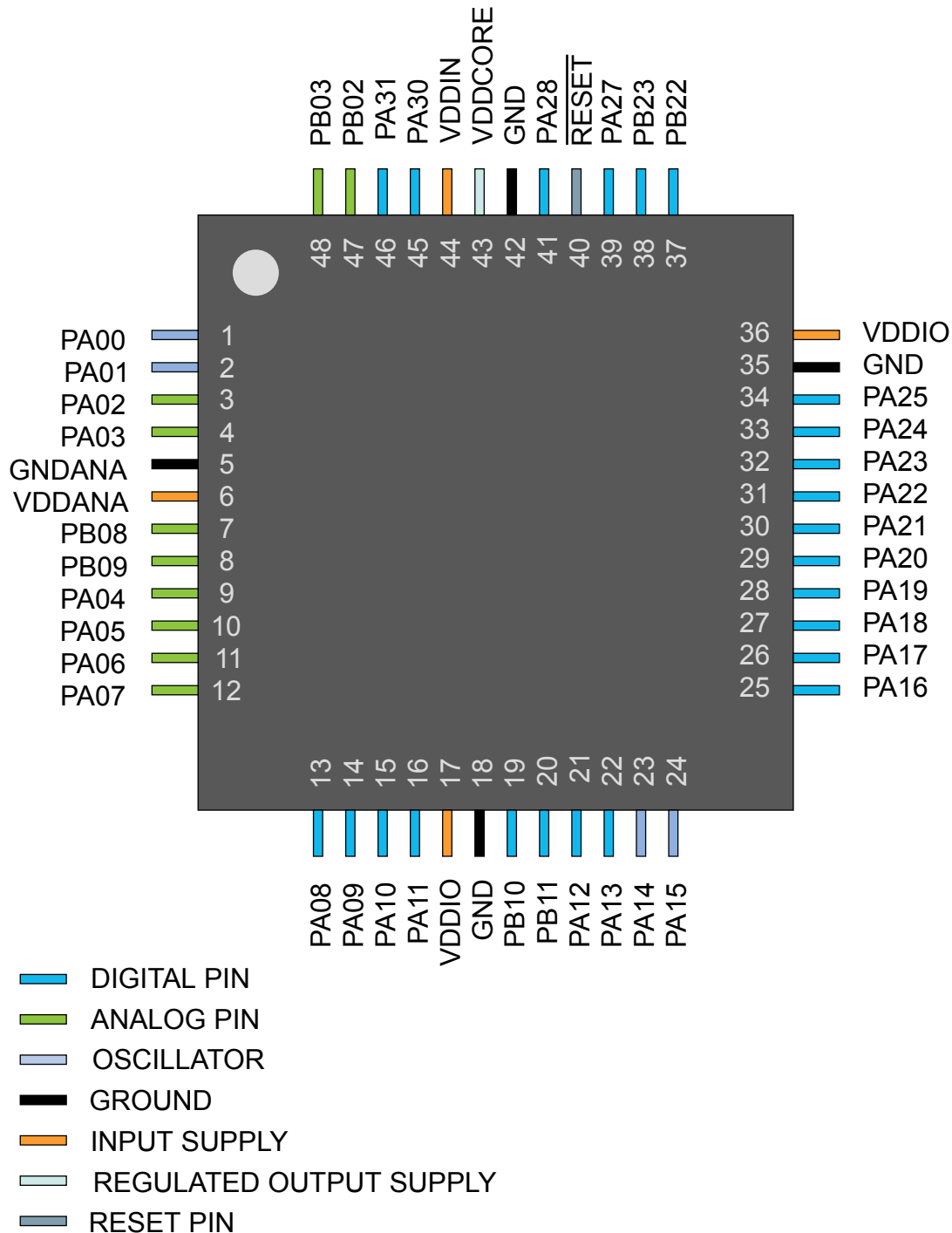
5.1. SAM D20J

5.1.1. QFN64 / TQFP64

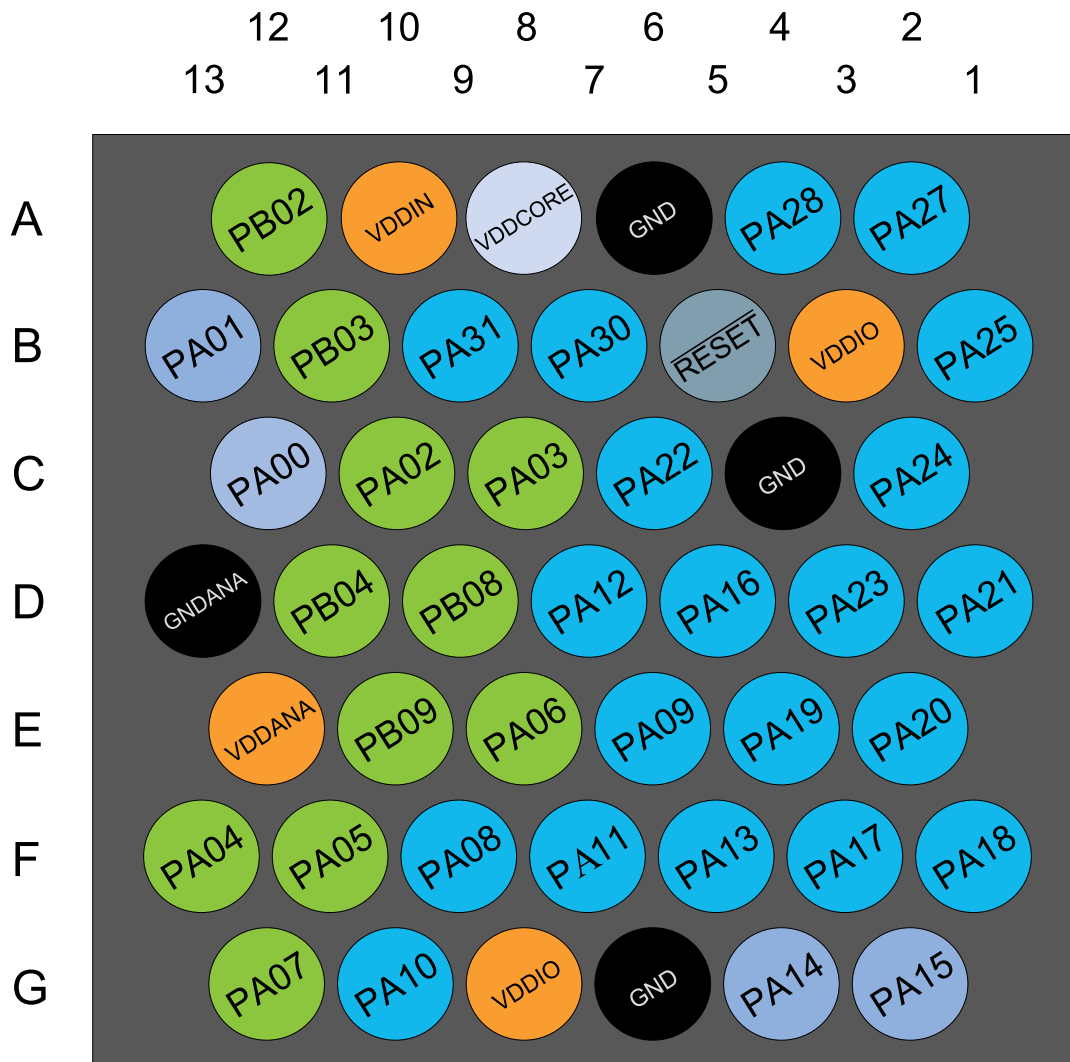


5.2. SAM D20G

5.2.1. QFN48 / TQFP48



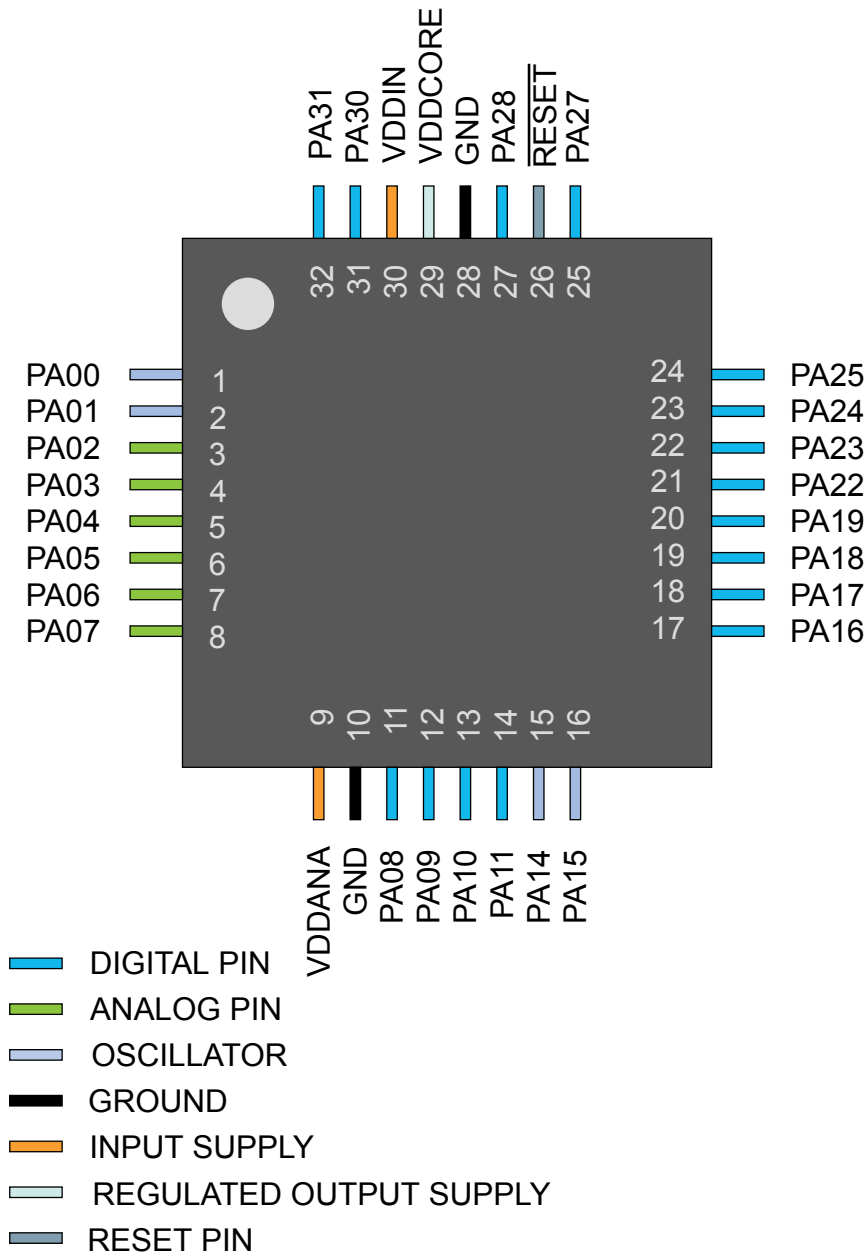
5.2.2. WLCSP45



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

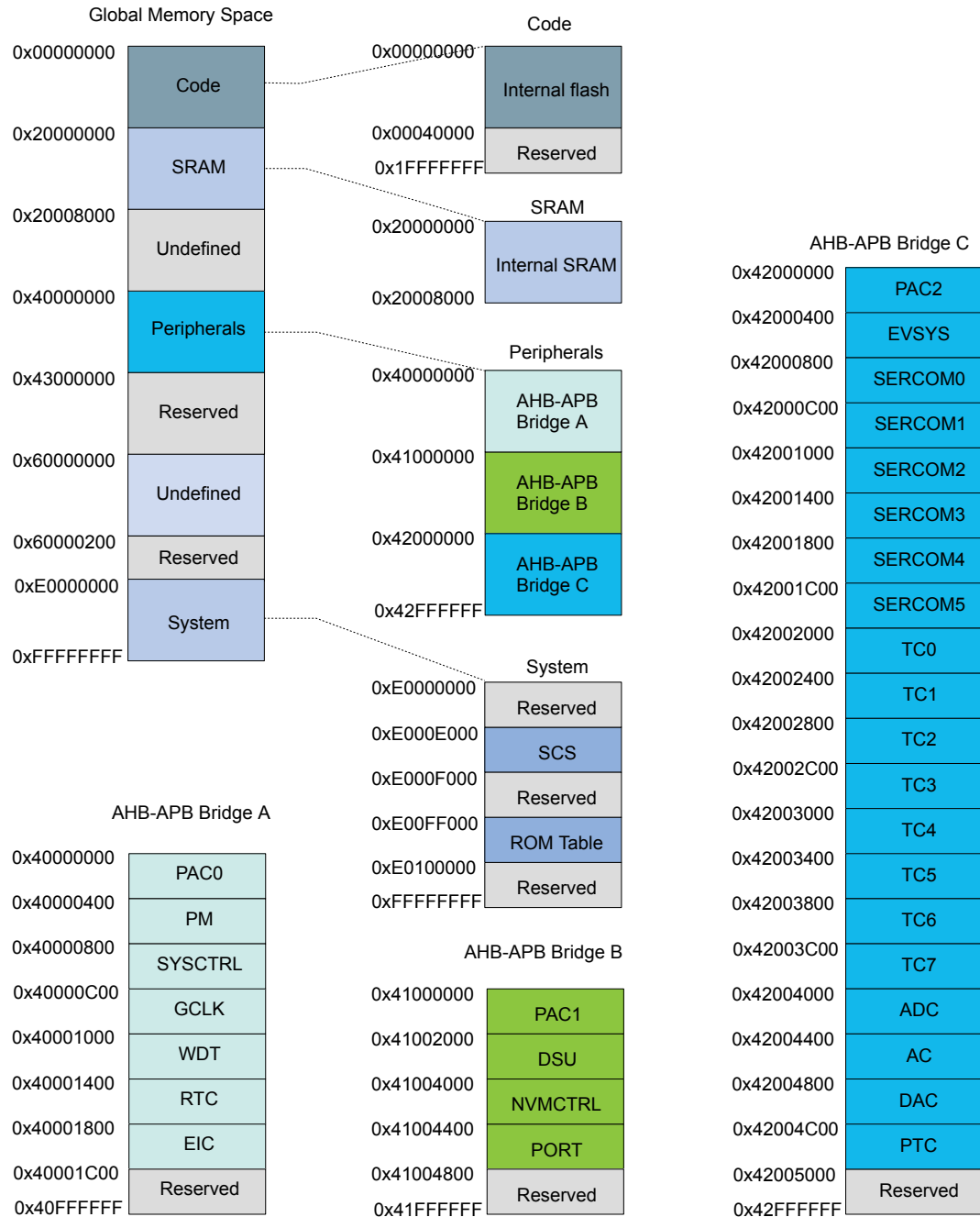
5.3. SAM D20E

5.3.1. QFN32 / TQFP32



6. Product Mapping

Figure 6-1. Product Mapping



This figure represents the full configuration of the SAM D20 device with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the [Configuration Summary](#) for details.

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBBx_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.

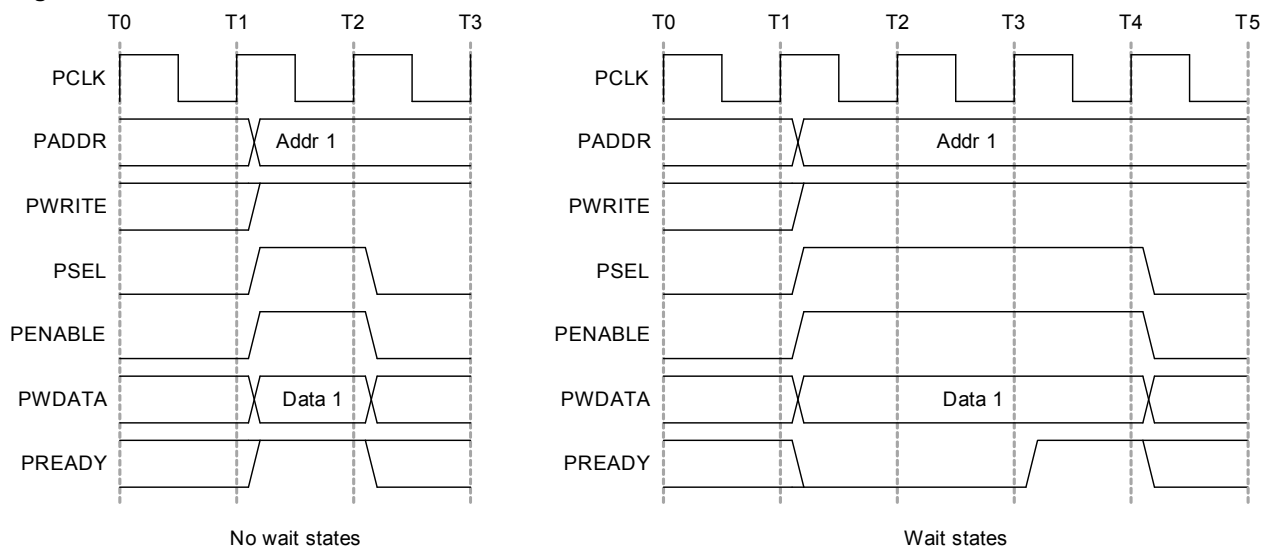
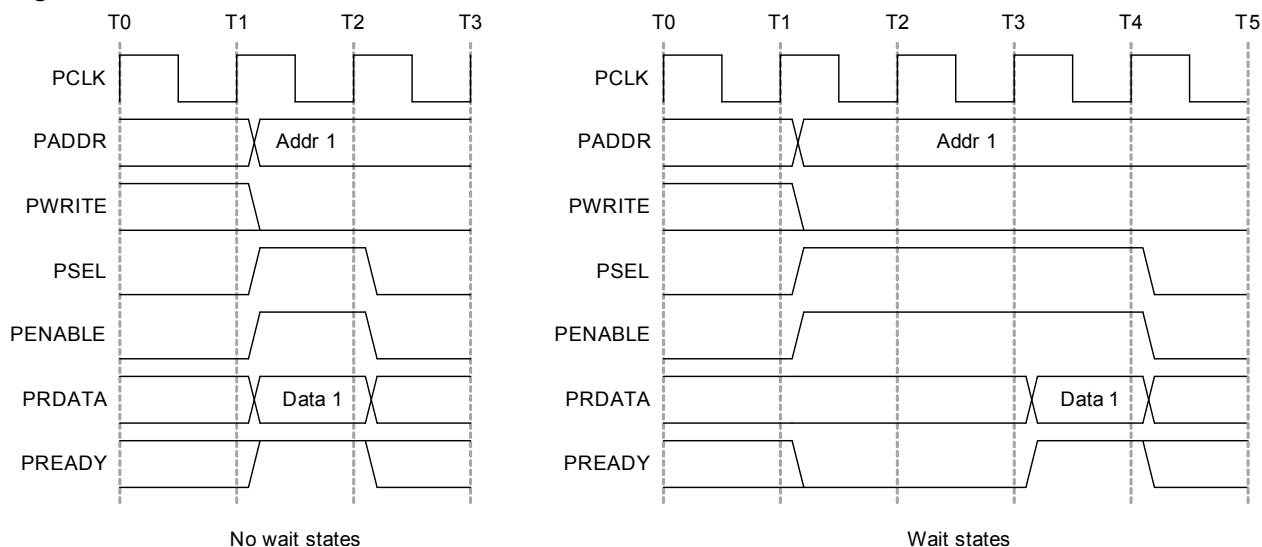


Figure 7-2. APB Read Access.



Related Links

[Product Mapping](#) on page 19

7.6. PAC - Peripheral Access Controller

7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled at reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

7.7.1.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.3.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.3.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYN	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

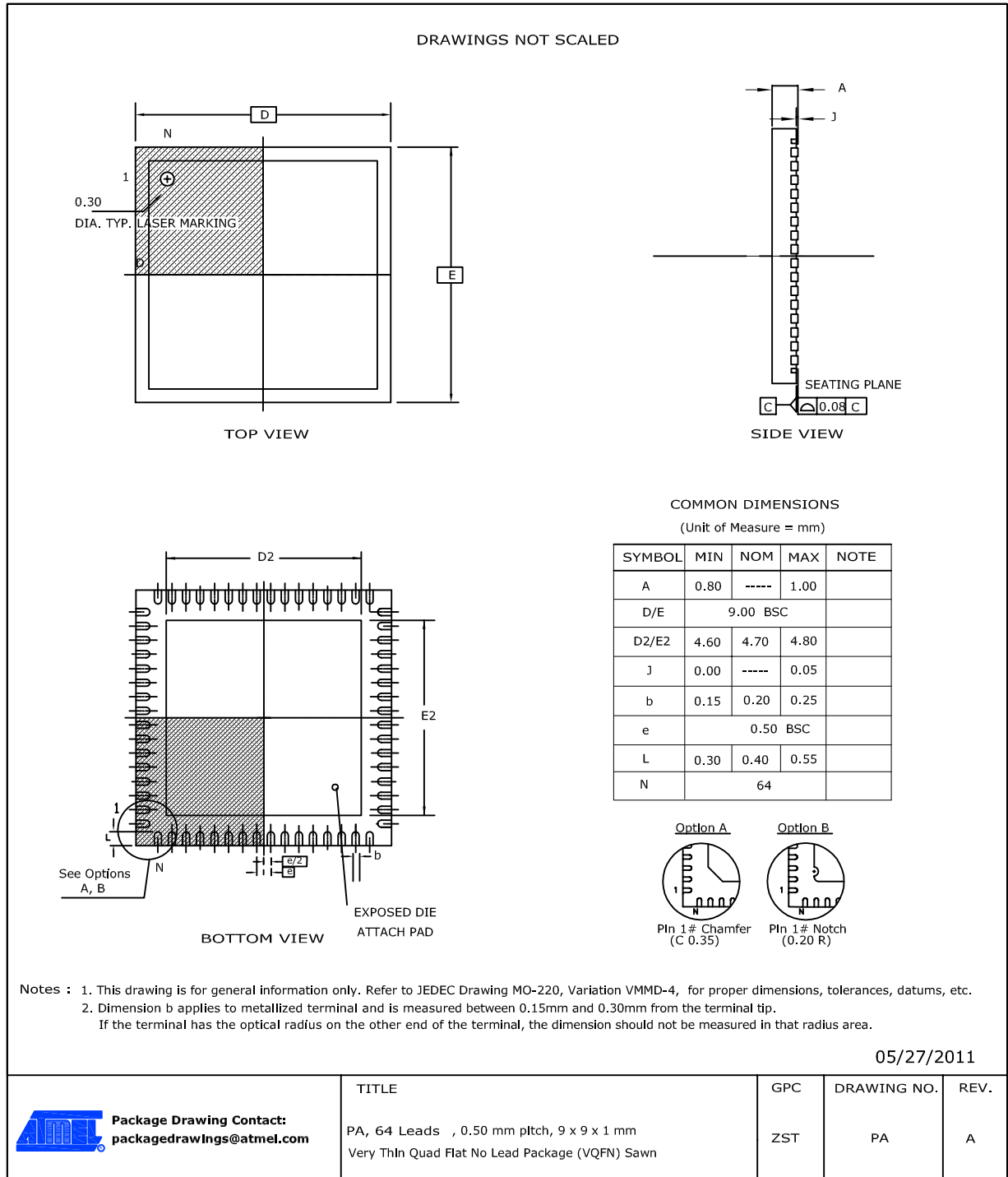
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Table 8-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.2. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

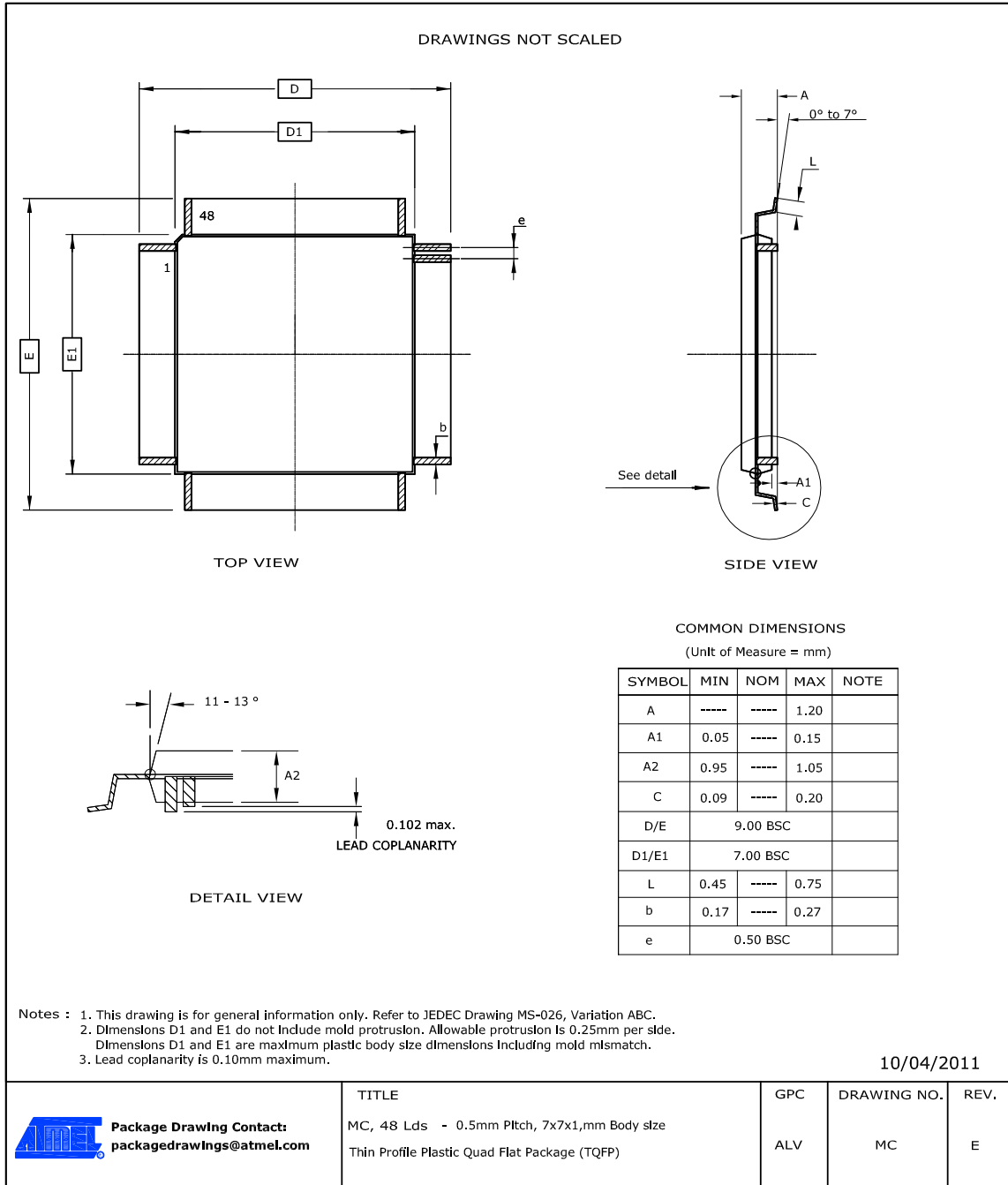
Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

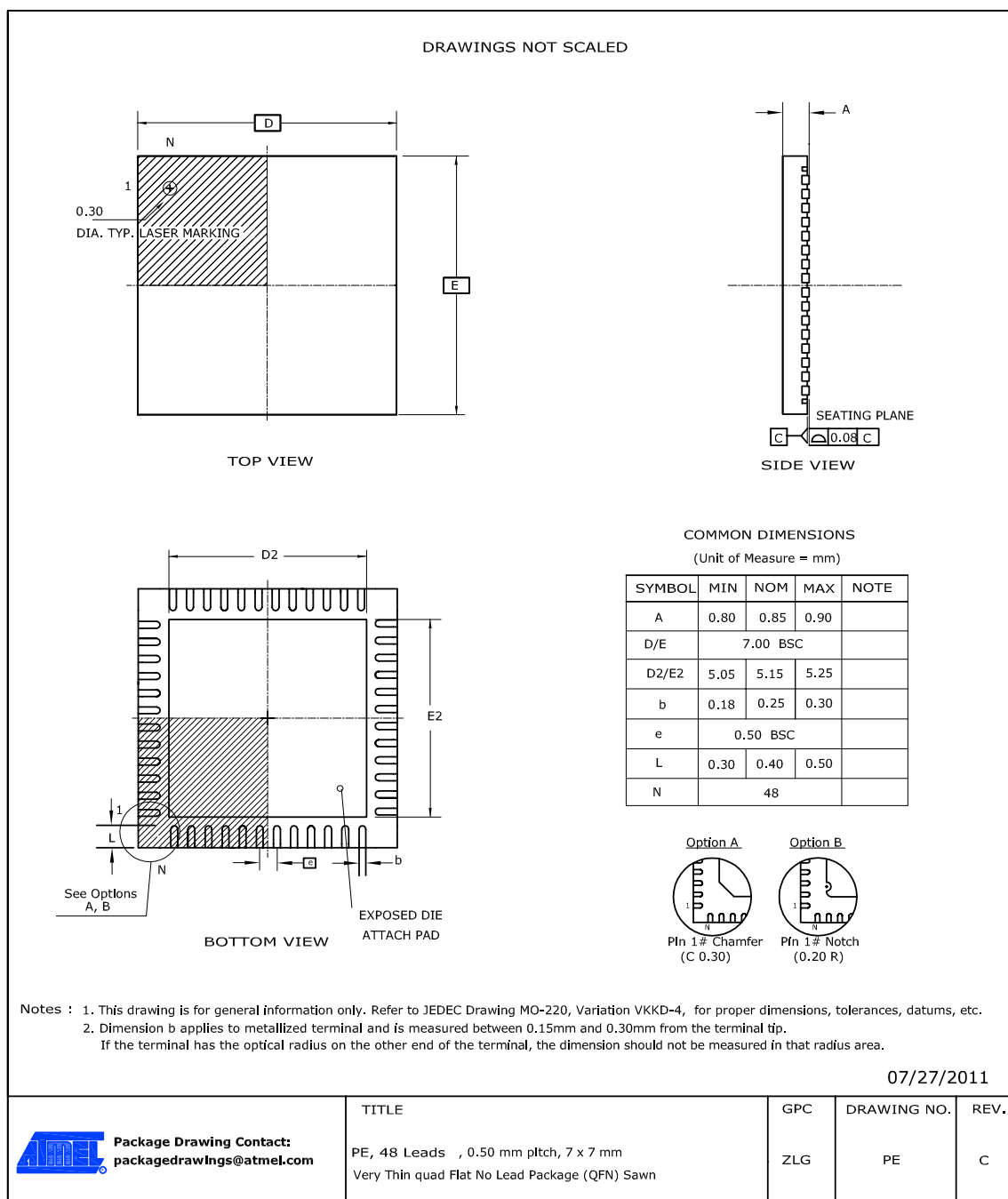
Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E8

8.2.4. 48 pin TQFP



8.2.5. 48 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-14. Device and Package Maximum Weight

140	mg
-----	----

Table 8-15. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

8.2.7. 32 pin TQFP

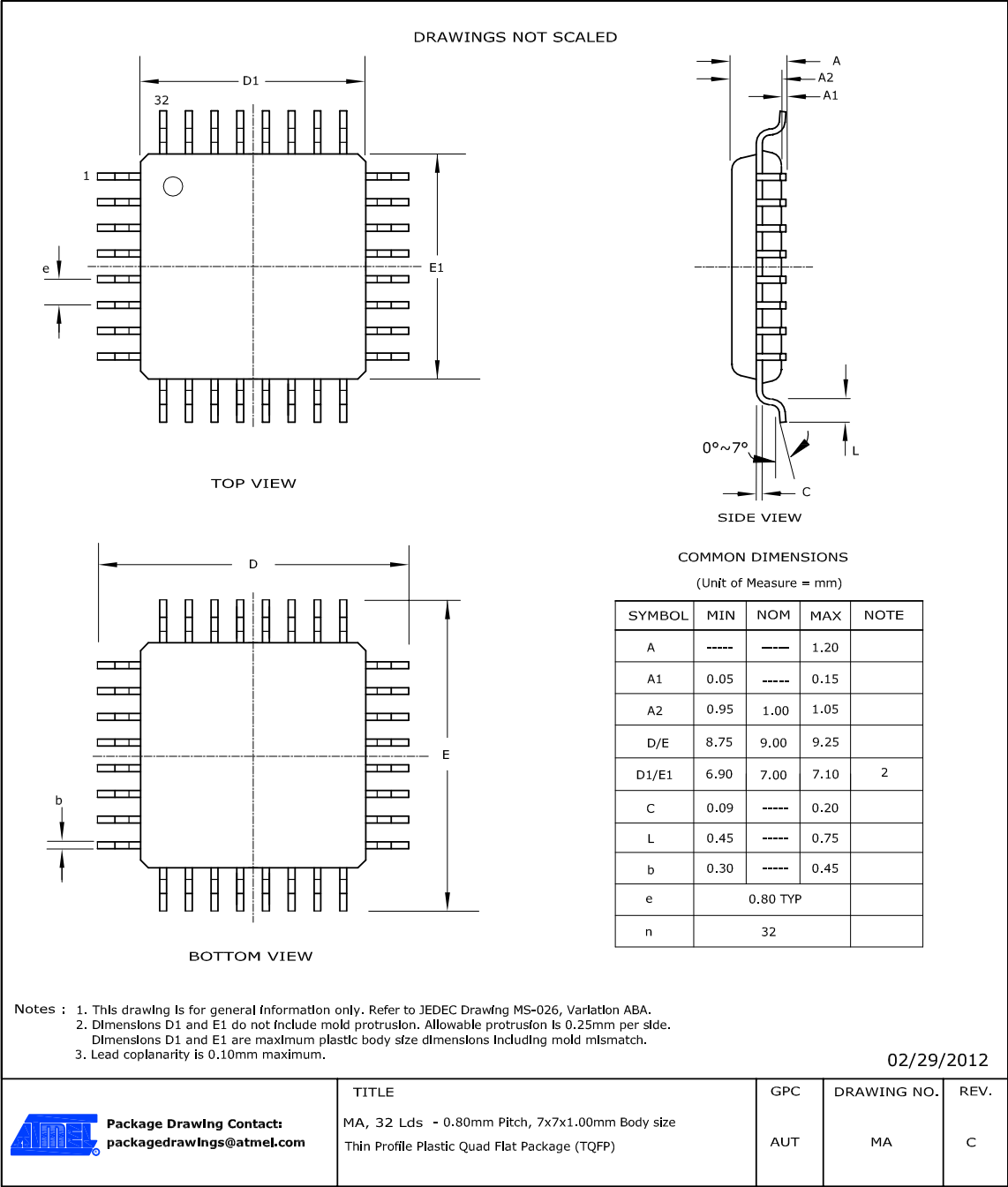


Table 8-20. Device and Package Maximum Weight

100	mg
-----	----

Table 8-21. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-24. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.9. 35 ball WLCSP

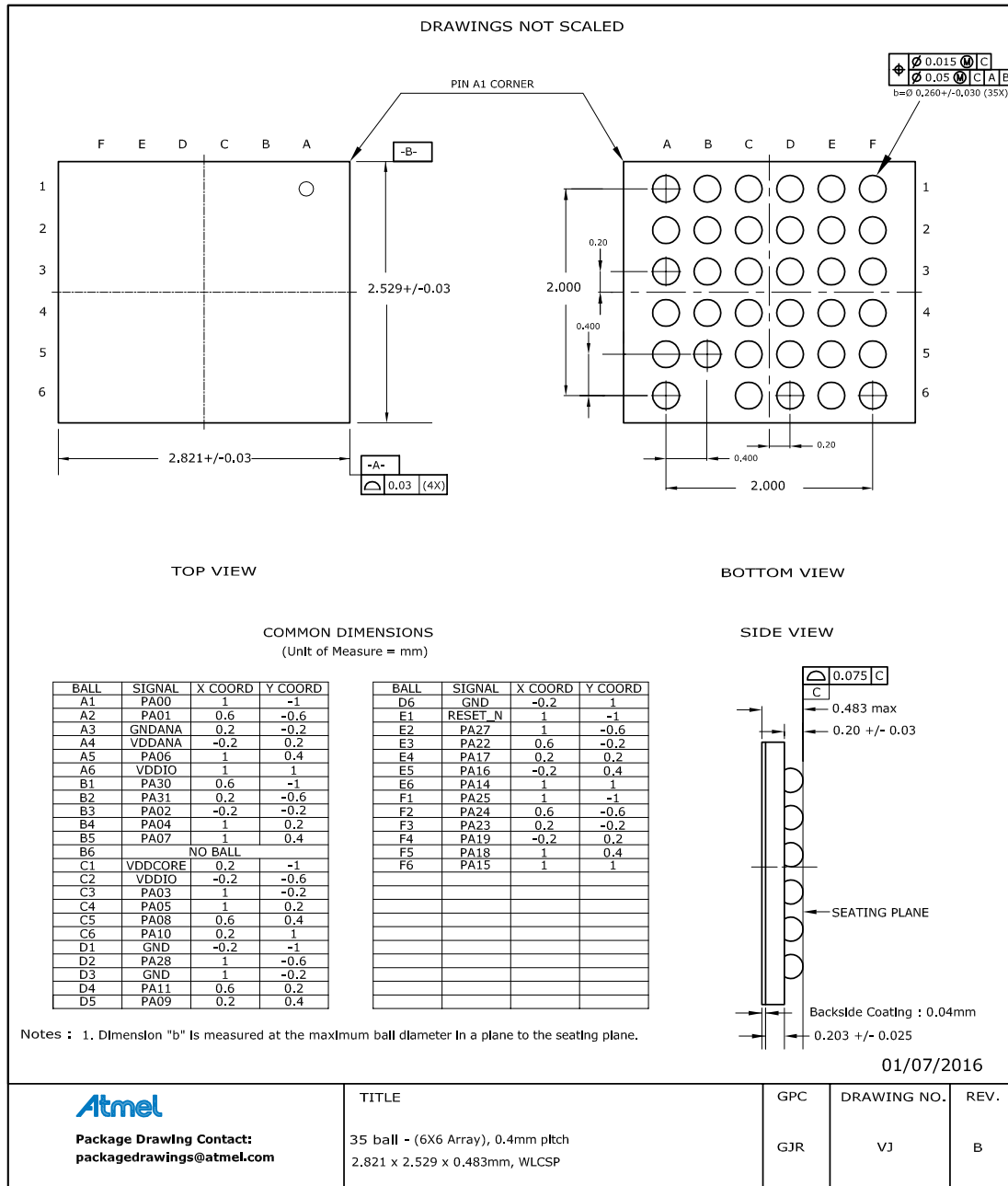


Table 8-26. Device and Package Maximum Weight

6.2	mg
-----	----