Microchip Technology - ATSAMD20J17A-AUT Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20j17a-aut

1. Description

The Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC) . The timer/counters can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 400kHz, up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

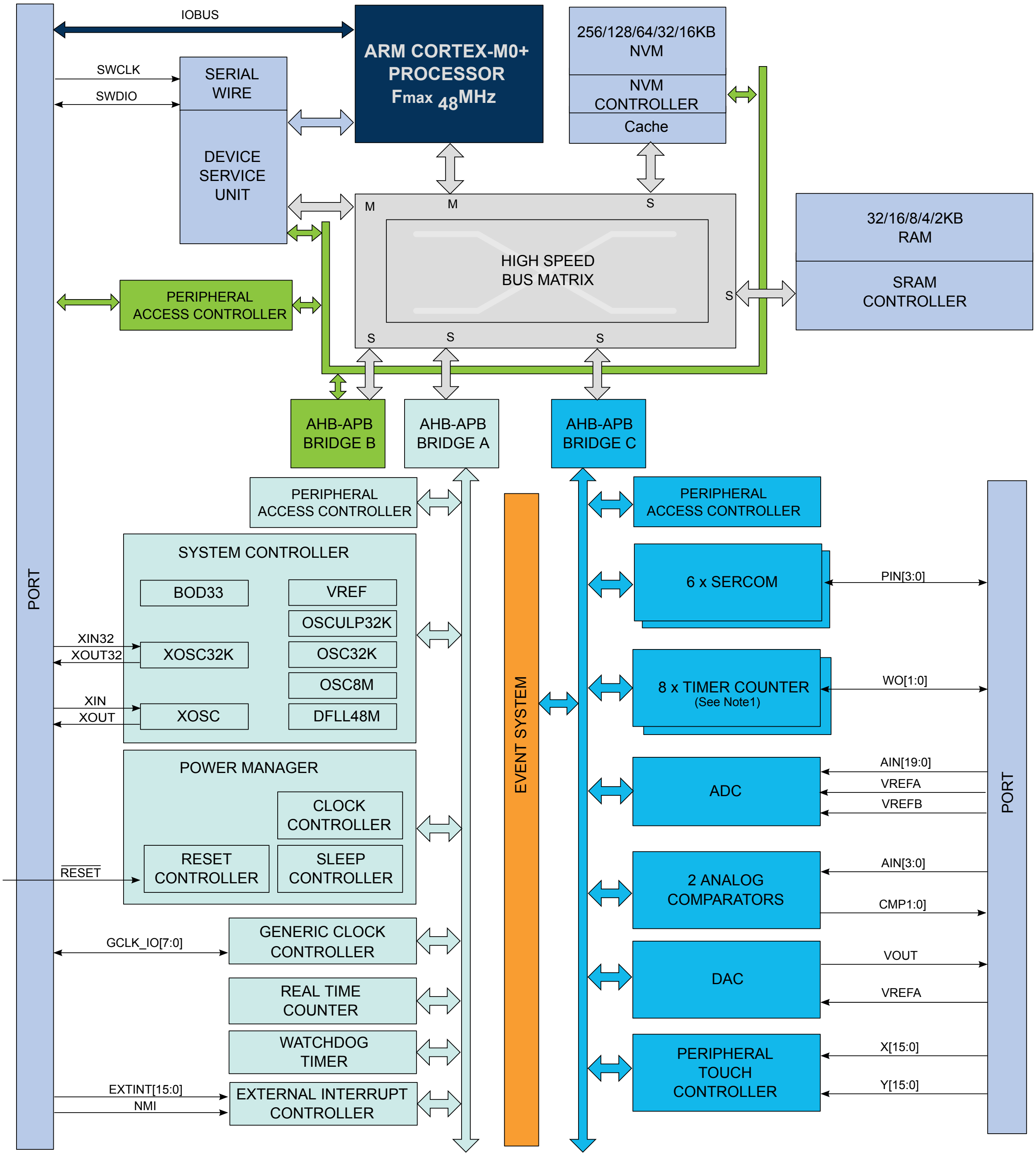
The SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E15A-AU	32K	4K	TQFP32	Tray
ATSAMD20E15A-AUT				Tape & Reel
ATSAMD20E15A-AN				Tray
ATSAMD20E15A-ANT				Tape & Reel
ATSAMD20E15A-MU			QFN32	Tray
ATSAMD20E15A-MUT				Tape & Reel
ATSAMD20E15A-MN				Tray
ATSAMD20E15A-MNT				Tape & Reel
ATSAMD20E16A-AU	64K	8K	TQFP32	Tray
ATSAMD20E16A-AUT				Tape & Reel
ATSAMD20E16A-AN				Tray
ATSAMD20E16A-AFT				Tape & Reel
ATSAMD20E16A-MU			QFN32	Tray
ATSAMD20E16A-MUT				Tape & Reel
ATSAMD20E16A-MN				Tray
ATSAMD20E16A-MNT				Tape & Reel
ATSAMD20E17A-AU	128K	16K	TQFP32	Tray
ATSAMD20E17A-AUT				Tape & Reel
ATSAMD20E17A-AN				Tray
ATSAMD20E17A-ANT				Tape & Reel
ATSAMD20E17A-MU			QFN32	Tray
ATSAMD20E17A-MUT				Tape & Reel
ATSAMD20E17A-MN				Tray
ATSAMD20E17A-MNT				Tape & Reel
ATSAMD20E18A-AU	256K	32K	TQFP32	Tray
ATSAMD20E18A-AUT				Tape & Reel
ATSAMD20E18A-AN				Tray
ATSAMD20E18A-AFT				Tape & Reel
ATSAMD20E18A-MU			QFN32	Tray
ATSAMD20E18A-MUT				Tape & Reel
ATSAMD20E18A-MN				Tray
ATSAMD20E18A-MNT				Tape & Reel

3.2. SAM D20G

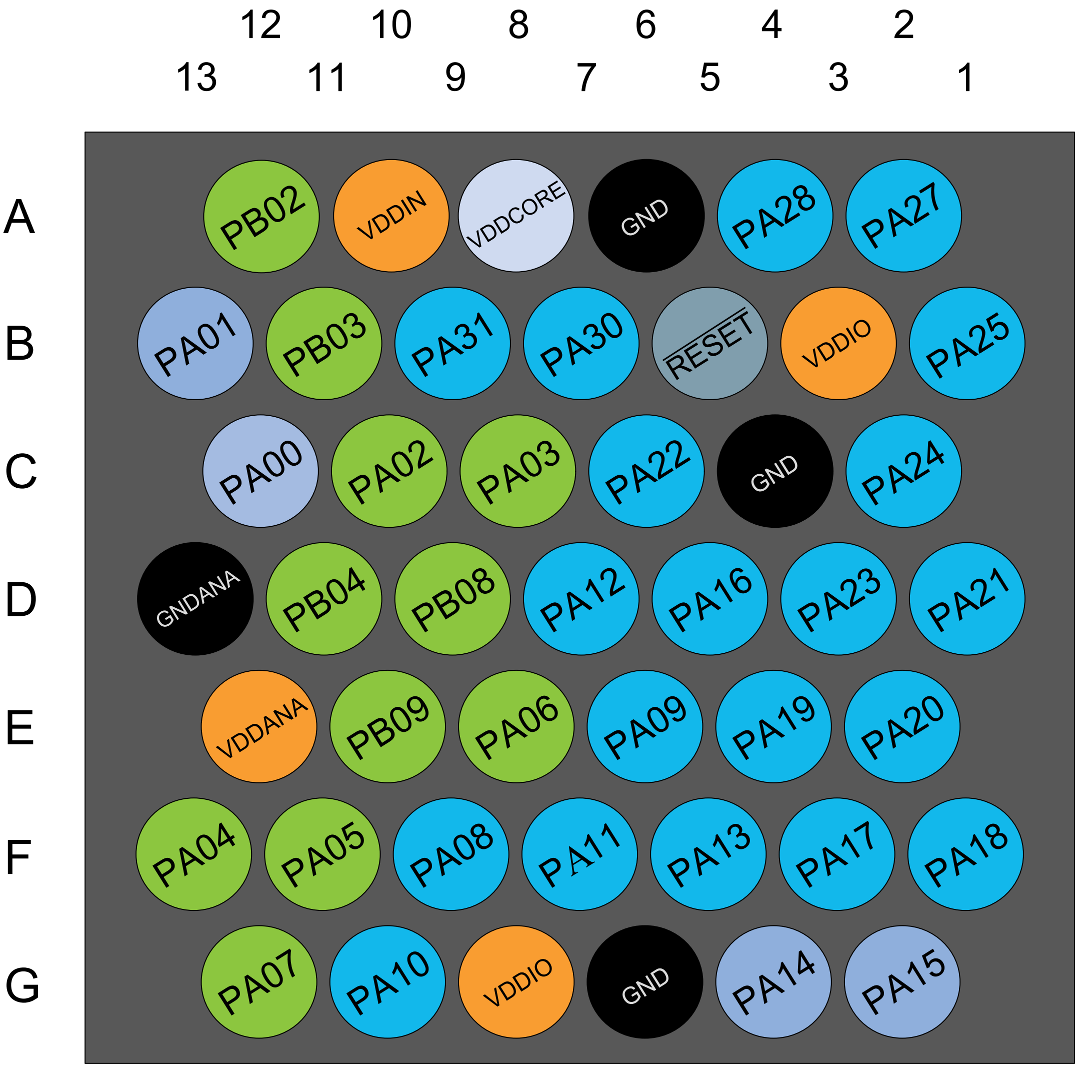
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G14A-AU	16K	2K	TQFP32	Tray
ATSAMD20G14A-AUT				Tape & Reel
ATSAMD20G14A-AN				Tray
ATSAMD20G14A-ANT				Tape & Reel
ATSAMD20G14A-MU			QFN32	Tray
ATSAMD20G14A-MUT				Tape & Reel
ATSAMD20G14A-MN				Tray
ATSAMD20G14A-MNT				Tape & Reel
ATSAMD20G15A-AU	32K	4K	TQFP48	Tray
ATSAMD20G15A-AUT				Tape & Reel
ATSAMD20G15A-AN				Tray
ATSAMD20G15A-ANT				Tape & Reel
ATSAMD20G15A-MU			QFN48	Tray
ATSAMD20G15A-MUT				Tape & Reel
ATSAMD20G15A-MN				Tray
ATSAMD20G15A-MNT				Tape & Reel
ATSAMD20G16A-AU	64K	8K	TQFP48	Tray
ATSAMD20G16A-AUT				Tape & Reel
ATSAMD20G16A-AN				Tray
ATSAMD20G16A-ANT				Tape & Reel
ATSAMD20G16A-MU			QFN48	Tray
ATSAMD20G16A-MUT				Tape & Reel
ATSAMD20G16A-MN				Tray
ATSAMD20G16A-MNT				Tape & Reel

4. Block Diagram



Note: 1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to *Peripherals Configuration Summary* for details.

5.2.2. WLCSP45

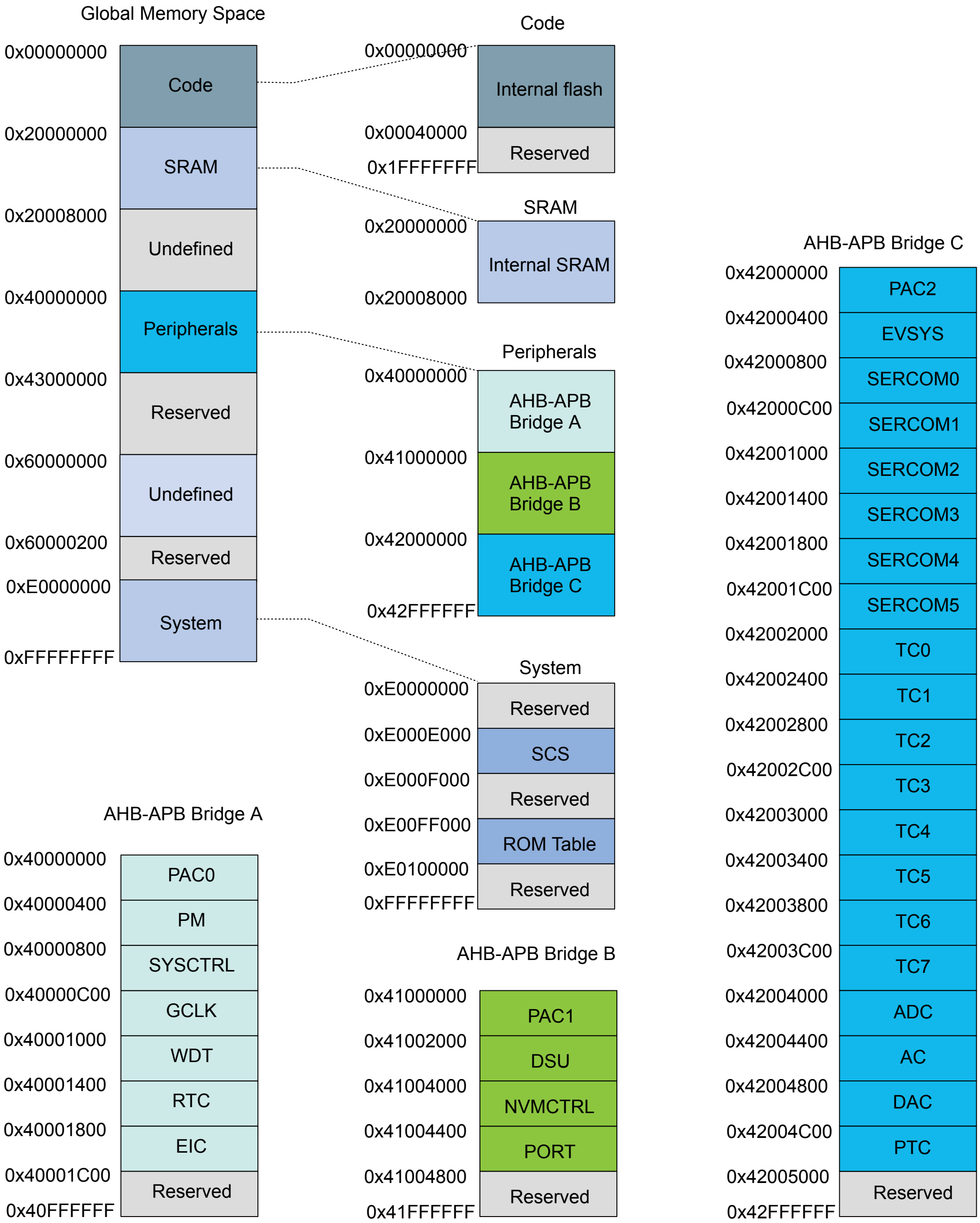


	13	12	11	10	9	8	7	6	5	4	3	2	1
A		PB02		VDDIN		VDDCORE		GND		PA28		PA27	
B	PA01		PB03		PA31		PA30		RESET		VDDIO		PA25
C		PA00		PA02		PA03		PA22		GND		PA24	
D	GNDANA		PB04		PB08		PA12		PA16		PA23		PA21
E		VDDANA		PB09		PA06		PA09		PA19		PA20	
F	PA04		PA05		PA08		PA11		PA13		PA17		PA18
G		PA07		PA10		VDDIO		GND		PA14		PA15	

- 🟦 DIGITAL PIN
- 🟩 ANALOG PIN
- ▭ OSCILLATOR
- ▬ GROUND
- 🟧 INPUT SUPPLY
- ▭ REGULATED OUTPUT SUPPLY
- ▭ RESET PIN

6. Product Mapping

Figure 6-1. Product Mapping



This figure represents the full configuration of the SAM D20 device with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the Configuration Summary for details.

  - The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (www.arm.com).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

7.1.3. Cortex-M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000 (see also Product Mapping)	Micro Trace Buffer (MTB)

7.1.4. I/O Interface

7.1.4.1. Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

7.1.4.2. Description

Direct access to PORT registers.

7.2. Nested Vector Interrupt Controller

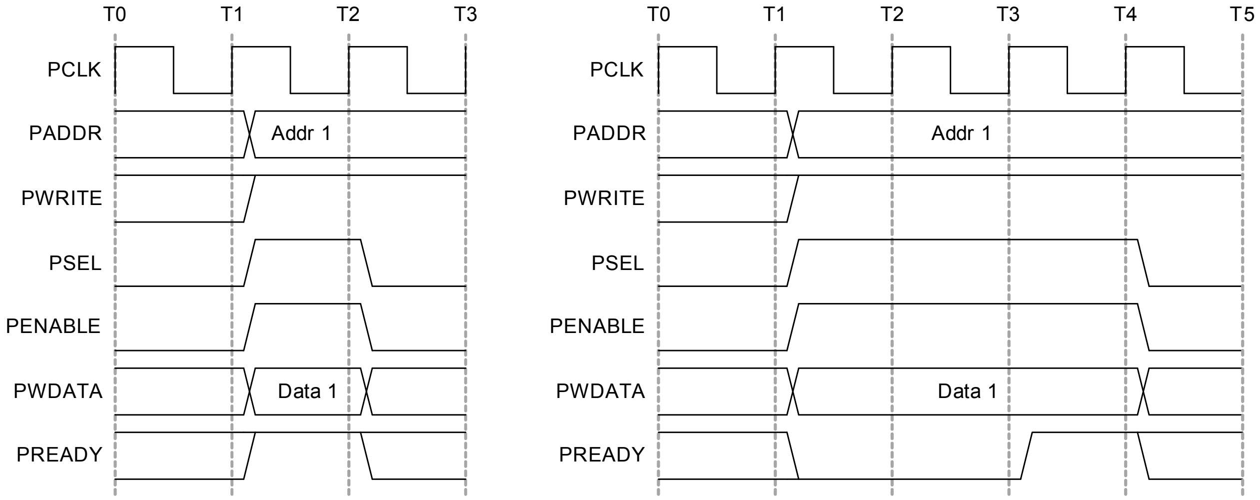
7.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM D20 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (www.arm.com).

7.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear

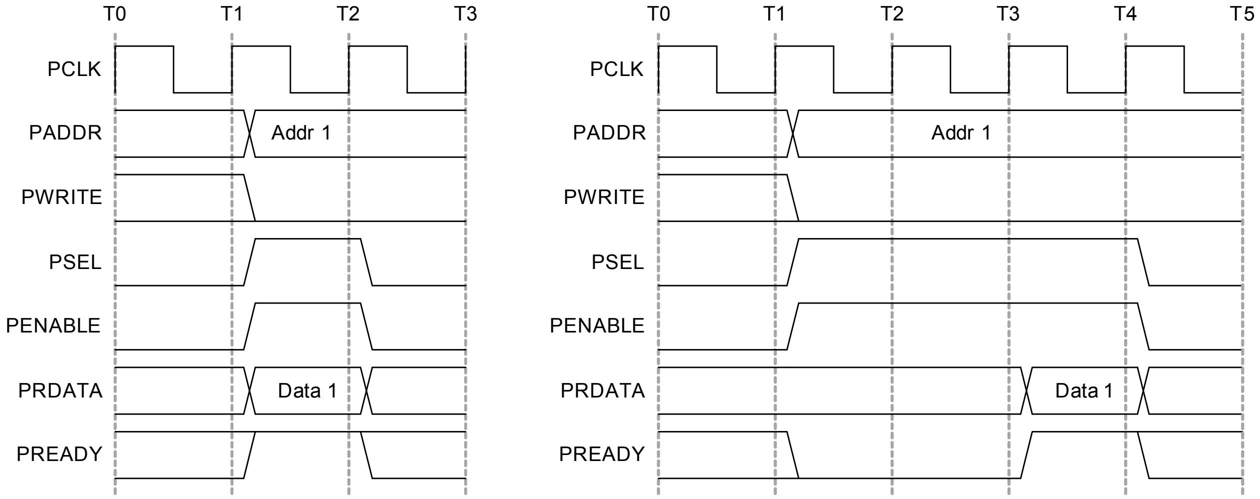
Figure 7-1. APB Write Access.



No wait states

Wait states

Figure 7-2. APB Read Access.



No wait states

Wait states

Related Links

Product Mapping on page 19

7.6. PAC - Peripheral Access Controller

7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled are reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.2.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000002
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		MTB			PORT	NVMCTRL	DSU	
Access		R/W			R/W	R/W	R/W	
Reset		0			0	0	1	

Bit 6 – MTB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.3.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.3.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

8. Packaging Information

8.1. Thermal Considerations

Related Links

Junction Temperature on page 39

8.1.1. Thermal Resistance Data

The following *table* summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	68.0°C/W	25.8°C/W
48-pin TQFP	78.8°C/W	12.3°C/W
64-pin TQFP	66.7°C/W	11.9°C/W
32-pin QFN	37.2°C/W	13.1°C/W
48-pin QFN	33.0°C/W	11.4°C/W
64-pin QFN	33.5°C/W	11.2°C/W
64-ball UFBGA	67.4°C/W	12.4°C/W
45-ball WLCSP	37.0°C/W	0.36°C/W

8.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

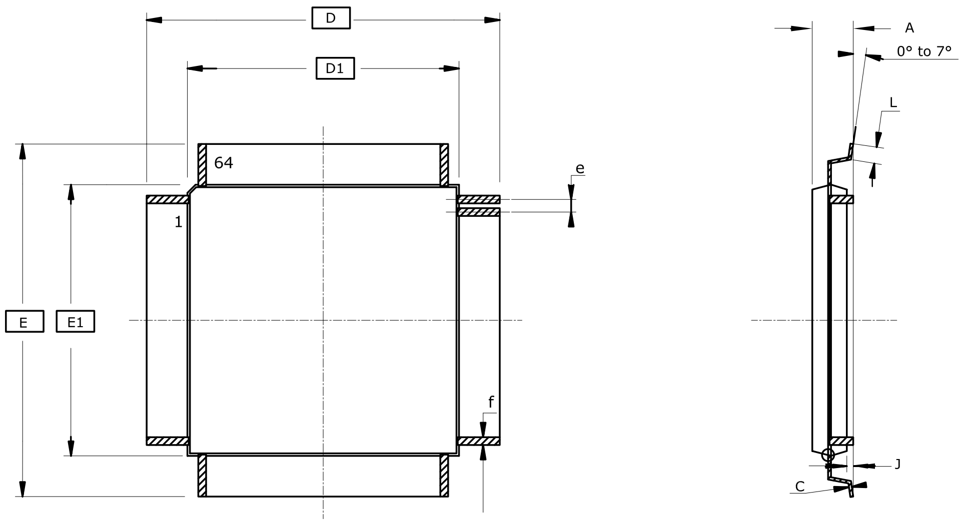
Related Links

Thermal Considerations on page 39

8.2. Package Drawings

8.2.1. 64 pin TQFP

DRAWINGS NOT SCALED



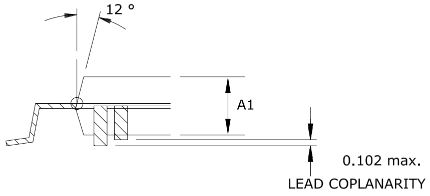
TOP VIEW

SIDE VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		



DETAIL VIEW

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	TITLE MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	GPC AIN	DRAWING NO. MF	REV. D

Table 8-2. Device and Package Maximum Weight

300	mg

Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-5. Device and Package Maximum Weight

200	mg

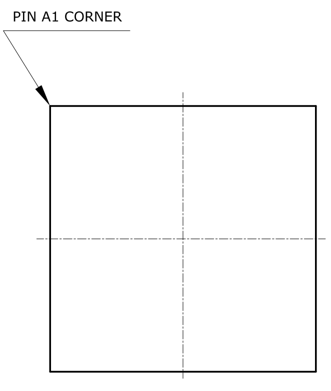
Table 8-6. Package Charateristics

Moisture Sensitivity Level	MSL3

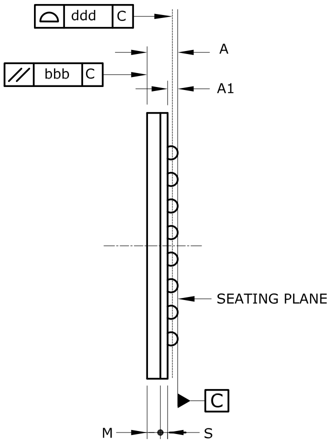
Table 8-7. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.3. 64-ball UFBGA



TOP VIEW

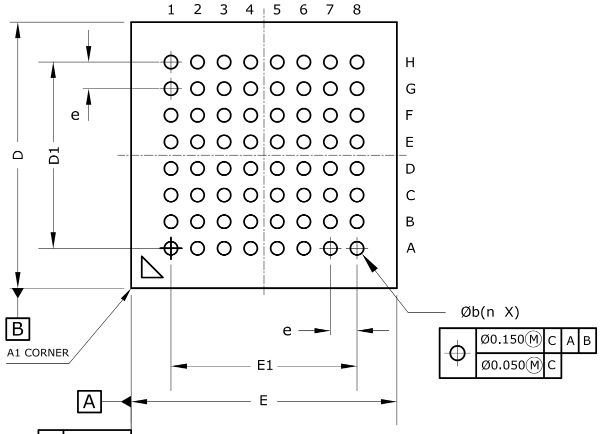


SIDE VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	0.650	
A1	0.140	-----	0.240	
E/D	5.00 / 5.00			
E1/D1	3.50 / 3.50			
b	0.200	-----	0.300	
e	Ball pitch : 0.500			
M	Mold thickness : 0.250 ref			
S	Subst thickness : 0.136 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.100			
ball diam	0.250			
n	64			



BOTTOM VIEW

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 8-8. Device and Package Maximum Weight

27.4	mg

Table 8-11. Device and Package Maximum Weight

140	mg

Table 8-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-13. Package Reference

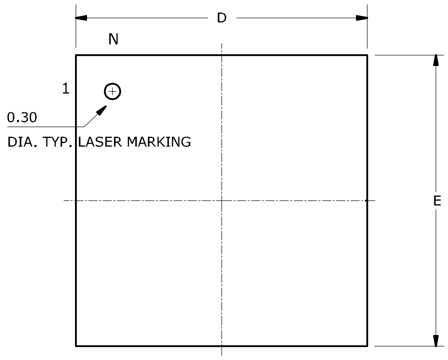
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Table 8-22. Package Reference

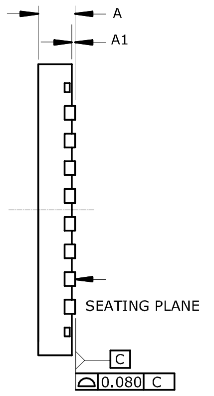
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.8. 32 pin QFN

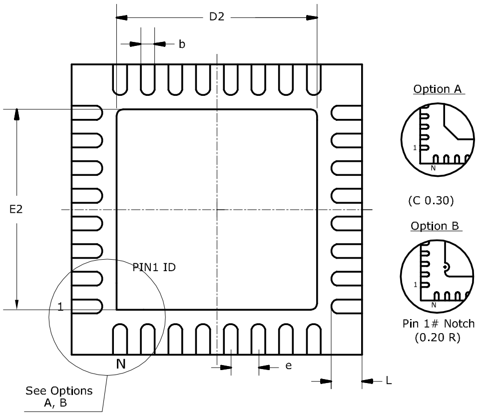
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	----	1.00	
A1	0.00	----	0.05	
D/E	5.00 BSC			
D2/E2	3.50	3.60	3.70	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e	0.50 BSC			
n	32			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-5, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

10/05/2015

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	PG, 32 Leads , 0.50mm pitch, 5x5x1.0mm Body Size Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZKV	PG	C

Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-23. Device and Package Maximum Weight

90	mg

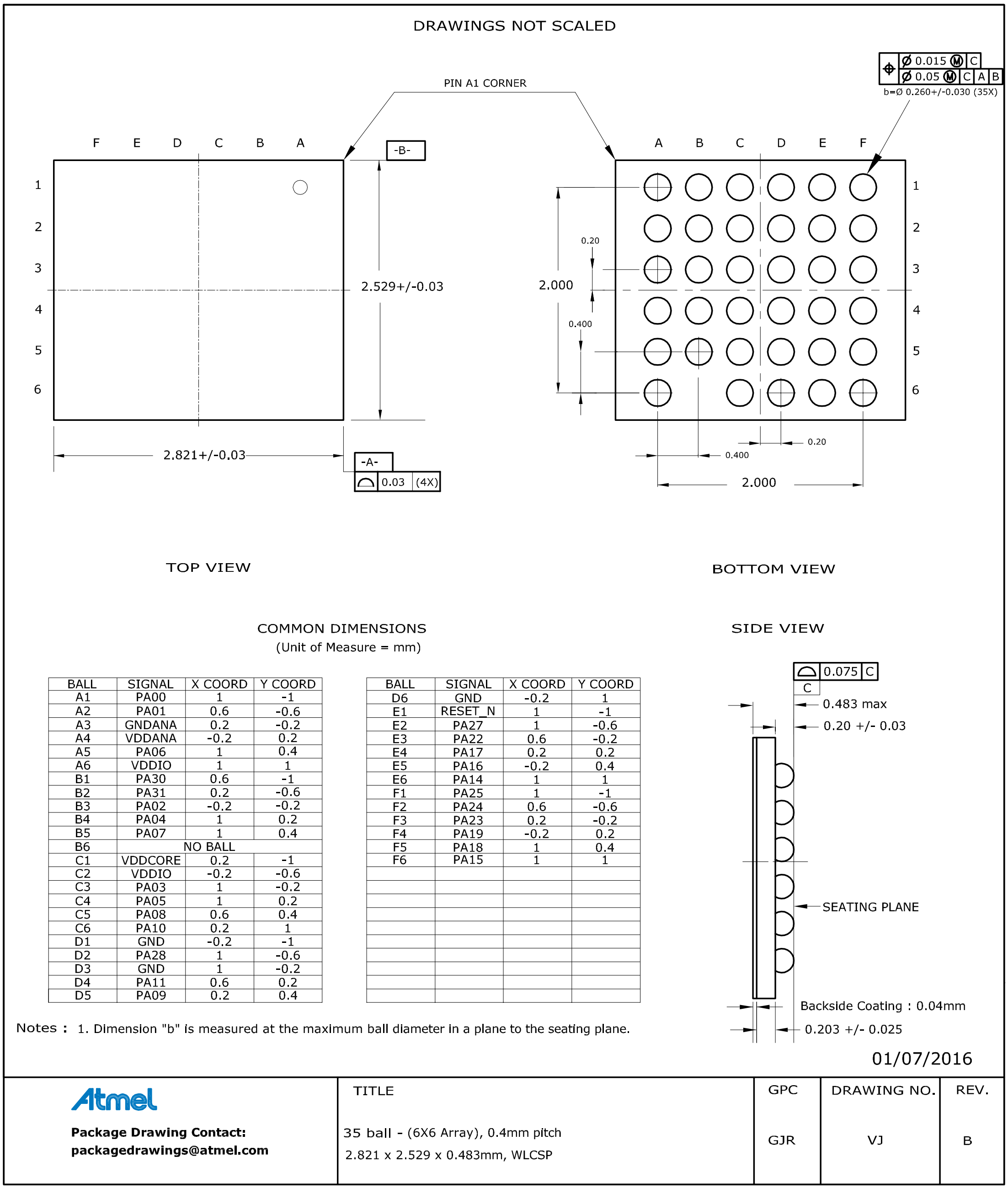
Table 8-24. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.9. 35 ball WLCSP



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PA00	1	-1
A2	PA01	0.6	-0.6
A3	GNDANA	0.2	-0.2
A4	VDDANA	-0.2	0.2
A5	PA06	1	0.4
A6	VDDIO	1	1
B1	PA30	0.6	-1
B2	PA31	0.2	-0.6
B3	PA02	-0.2	-0.2
B4	PA04	1	0.2
B5	PA07	1	0.4
B6	NO BALL		
C1	VDDCORE	0.2	-1
C2	VDDIO	-0.2	-0.6
C3	PA03	1	-0.2
C4	PA05	1	0.2
C5	PA08	0.6	0.4
C6	PA10	0.2	1
D1	GND	-0.2	-1
D2	PA28	1	-0.6
D3	GND	1	-0.2
D4	PA11	0.6	0.2
D5	PA09	0.2	0.4

BALL	SIGNAL	X COORD	Y COORD
D6	GND	-0.2	1
E1	RESET_N	1	-1
E2	PA27	1	-0.6
E3	PA22	0.6	-0.2
E4	PA17	0.2	0.2
E5	PA16	-0.2	0.4
E6	PA14	1	1
F1	PA25	1	-1
F2	PA24	0.6	-0.6
F3	PA23	0.2	-0.2
F4	PA19	-0.2	0.2
F5	PA18	1	0.4
F6	PA15	1	1

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

01/07/2016

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	35 ball - (6X6 Array), 0.4mm pitch 2.821 x 2.529 x 0.483mm, WLCSP	GJR	VJ	B

Table 8-26. Device and Package Maximum Weight

6.2	mg

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-29.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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