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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

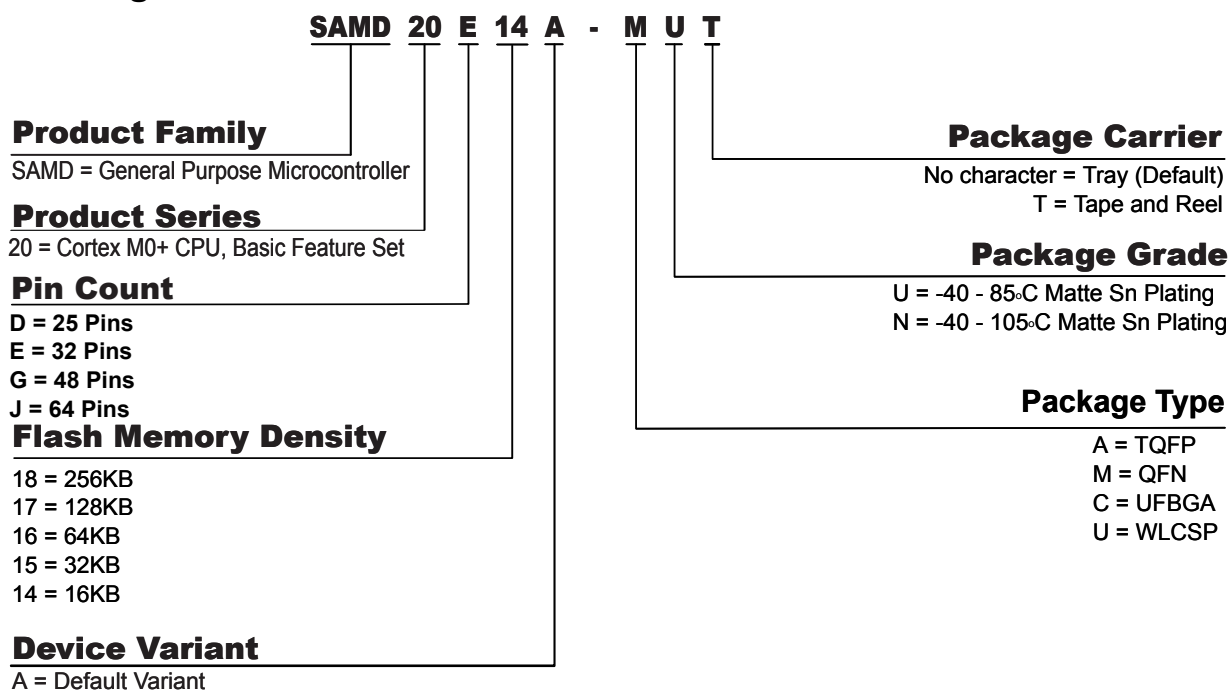
Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I ² C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 52 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 20x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-UFBGA |
| Supplier Device Package | 64-UFBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd20j18a-cnt |

2. Configuration Summary

| | SAM D20J | SAM D20G | SAM D20E |
|---|---|---------------------------------------|---------------------------------------|
| Pins | 64 | 48 | 32 |
| General Purpose I/O-pins (GPIOs) | 52 | 38 | 26 |
| Flash | 256/128/64/32KB | 256/128/64/32KB | 256/128/64/32KB |
| SRAM | 32/16/8/4/2KB | 32/16/8/4/2KB | 32/16/8/4/2KB |
| Timer Counter (TC) instances | 8 | 6 | 6 |
| Waveform output channels per TC instance | 2 | 2 | 2 |
| Serial Communication Interface (SERCOM) instances | 6 | 6 | 4 |
| Analog-to-Digital Converter (ADC) channels | 20 | 14 | 10 |
| Analog Comparators (AC) | 2 | 2 | 2 |
| Digital-to-Analog Converter (DAC) channels | 1 | 1 | 1 |
| Real-Time Counter (RTC) | Yes | Yes | Yes |
| RTC alarms | 1 | 1 | 1 |
| RTC compare values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values |
| External Interrupt lines | 16 | 16 | 16 |
| Peripheral Touch Controller (PTC) X and Y lines | 16x16 | 12x10 | 10x6 |
| Maximum CPU frequency | 48MHz | | |
| Packages | QFN TQFP UFBGA | QFN TQFP WLCSP | QFN TQFP |
| Oscillators | 32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) | | |
| Event System channels | 8 | 8 | 8 |
| SW Debug Interface | Yes | Yes | Yes |
| Watchdog Timer (WDT) | Yes | Yes | Yes |

3. Ordering Information



3.1. SAM D20E

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|------------------|---------------|--------------|---------|--------------|
| ATSAMD20E14A-AU | 16K | 2K | TQFP32 | Tray |
| ATSAMD20E14A-AUT | | | | Tape & Reel |
| ATSAMD20E14A-AN | | | | Tray |
| ATSAMD20E14A-ANT | | | | Tape & Reel |
| ATSAMD20E14A-MU | | | QFN32 | Tray |
| ATSAMD20E14A-MUT | | | | Tape & Reel |
| ATSAMD20E14A-MN | | | | Tray |
| ATSAMD20E14A-MNT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|------------------|---------------|--------------|---------|--------------|
| ATSAMD20J18A-AU | 256K | 32K | TQFP64 | Tray |
| ATSAMD20J18A-AUT | | | | Tape & Reel |
| ATSAMD20J18A-AN | | | | Tray |
| ATSAMD20J18A-ANT | | | | Tape & Reel |
| ATSAMD20J18A-MU | | | QFN64 | Tray |
| ATSAMD20J18A-MUT | | | | Tape & Reel |
| ATSAMD20J18A-MN | | | | Tray |
| ATSAMD20J18A-MNT | | | | Tape & Reel |
| ATSAMD20J18A-CU | | | UFBGA64 | Tray |
| ATSAMD20J18A-CUT | | | | Tape & Reel |

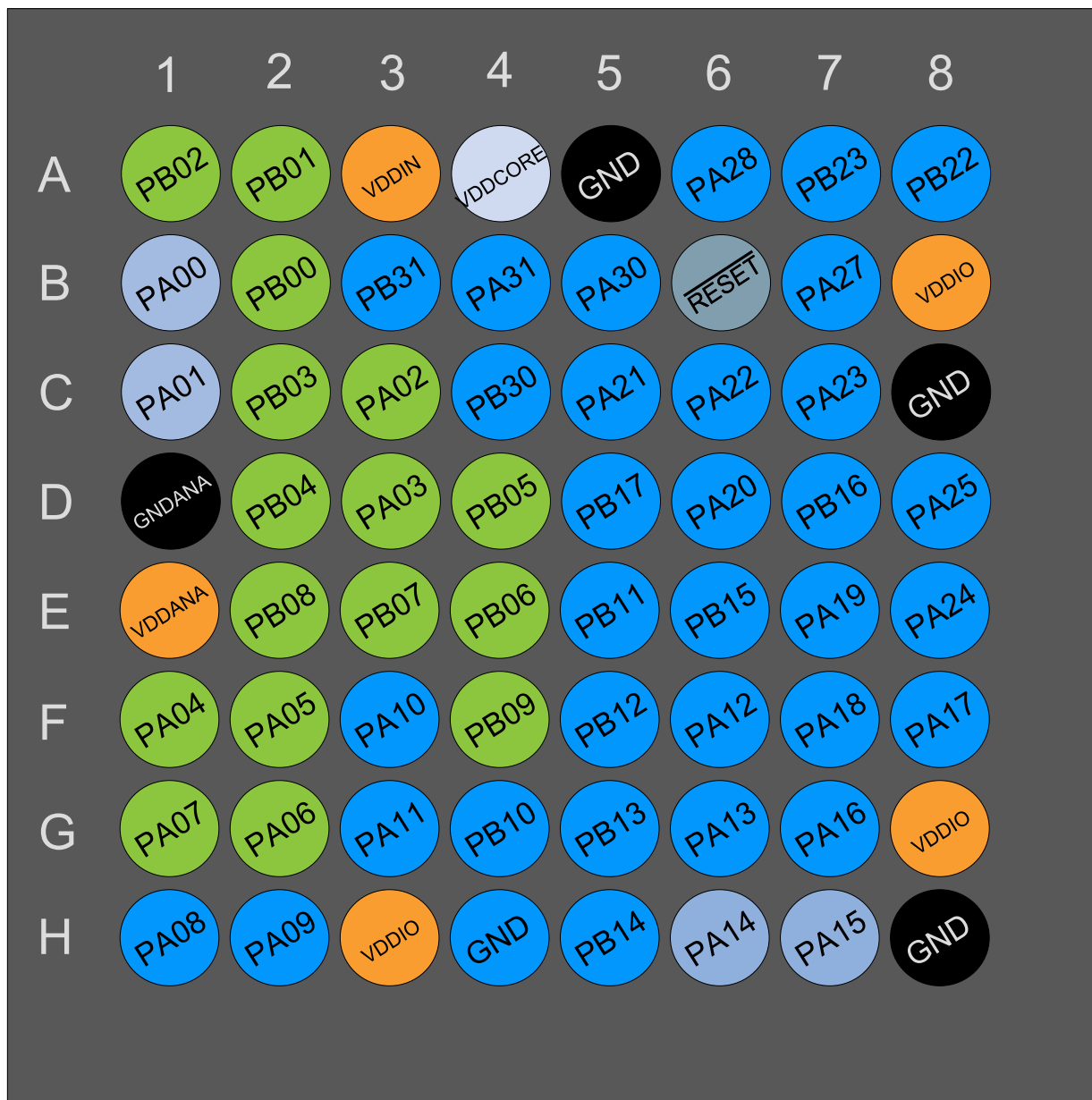
3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-1. Device Identification Values

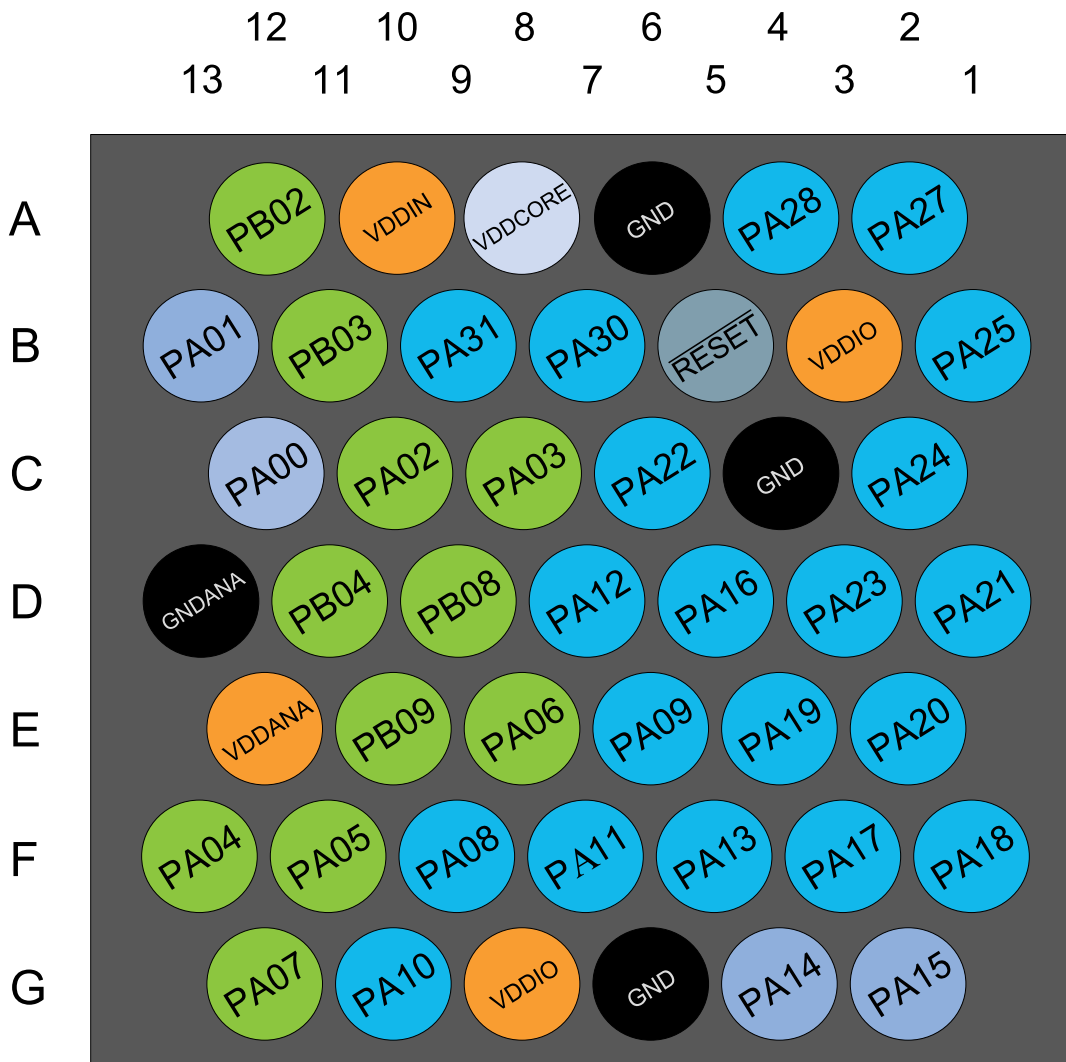
| Device Variant | DID.DEVSEL | Device ID (DID) |
|----------------|------------|-----------------|
| SAMD20J18C | 0x00 | 0x10001300 |
| SAMD20J18A | 0x00 | 0x10001300 |
| SAMD20J17A | 0x01 | 0x10001301 |
| SAMD20J16A | 0x02 | 0x10001302 |
| SAMD20J15A | 0x03 | 0x10001303 |
| SAMD20J14A | 0x04 | 0x10001304 |
| SAMD20G18A | 0x05 | 0x10001305 |
| SAMD20G17A | 0x06 | 0x10001306 |
| SAMD20G16A | 0x07 | 0x10001307 |
| SAMD20G15A | 0x08 | 0x10001308 |
| SAMD20G14A | 0x09 | 0x10001309 |
| SAMD20E18A | 0x0A | 0x1000130A |
| SAMD20E17A | 0x0B | 0x1000130B |
| SAMD20E16A | 0x0C | 0x1000130C |
| SAMD20E15A | 0x0D | 0x1000130D |

5.1.2. UFBGA64



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

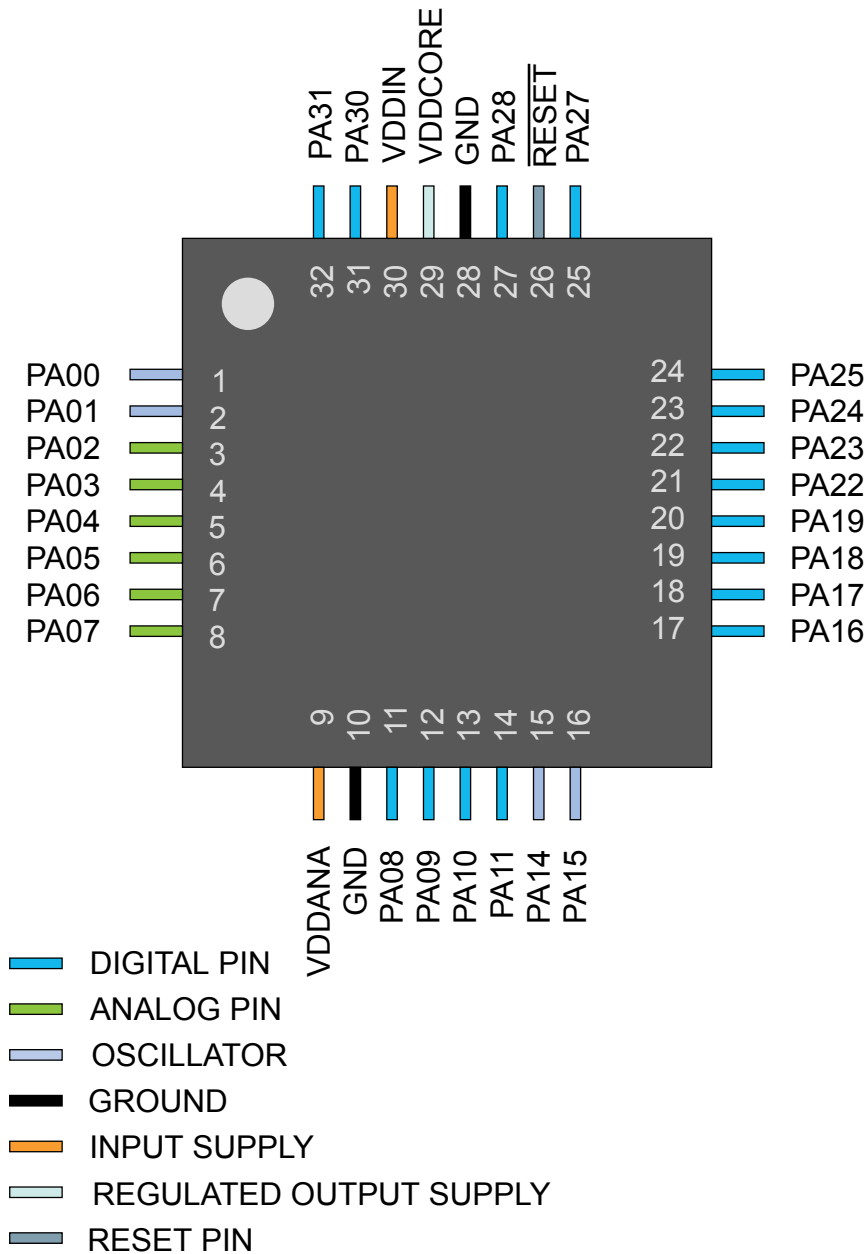
5.2.2. WLCSP45



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

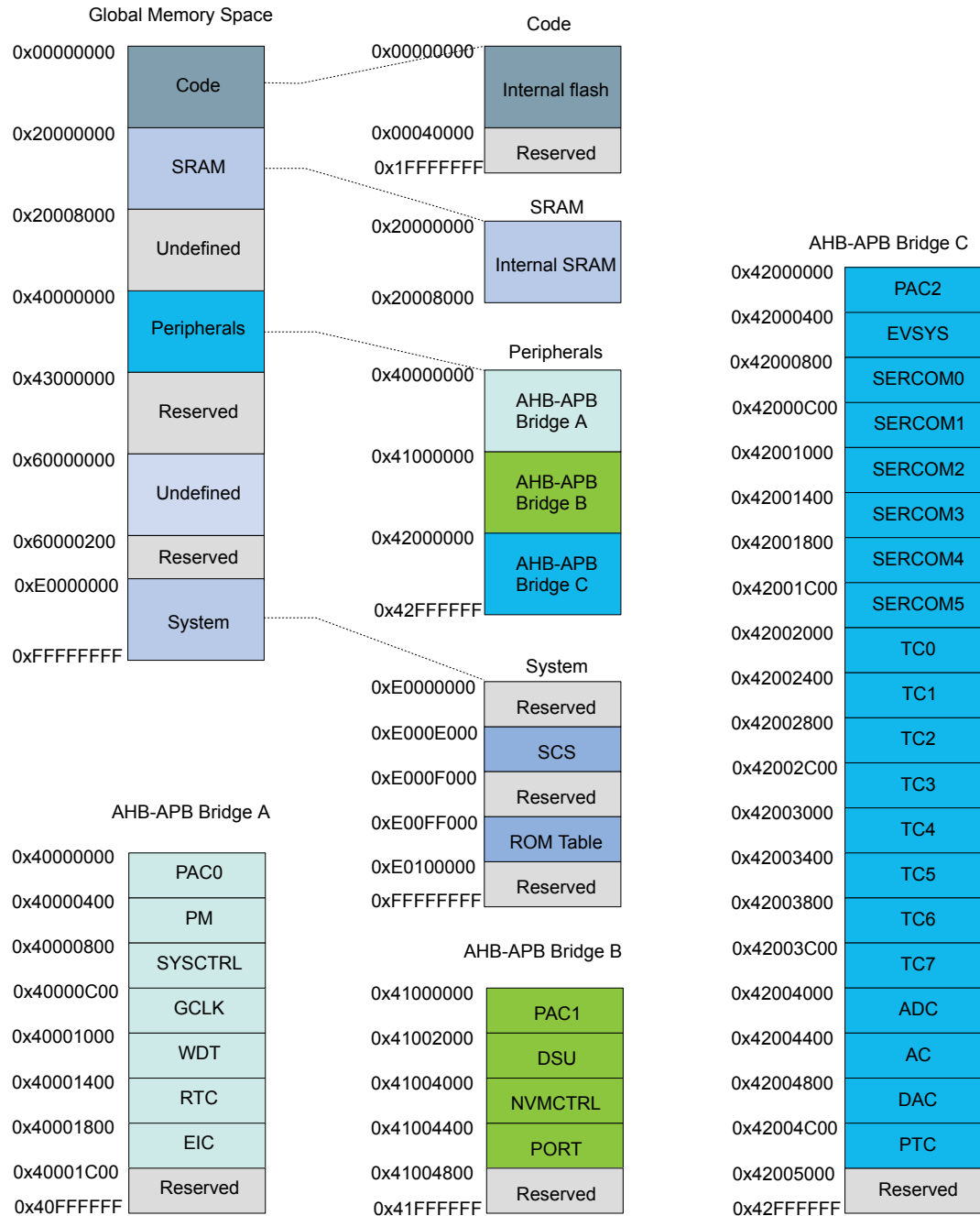
5.3. SAM D20E

5.3.1. QFN32 / TQFP32



6. Product Mapping

Figure 6-1. Product Mapping



This figure represents the full configuration of the SAM D20 device with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the [Configuration Summary](#) for details.

7. Processor And Architecture

7.1. Cortex M0+ Processor

The SAM D20 implements the ARM[®] Cortex[®]-M0+ processor, based on the ARMv6 Architecture and Thumb[®]-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to <http://www.arm.com>.

7.1.1. Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration

| Features | Configurable option | Device configuration |
|----------------------------------|------------------------------|-----------------------|
| Interrupts | External interrupts 0-32 | 28 |
| Data endianness | Little-endian or big-endian | Little-endian |
| SysTick timer | Present or absent | Present |
| Number of watchpoint comparators | 0, 1, 2 | 2 |
| Number of breakpoint comparators | 0, 1, 2, 3, 4 | 4 |
| Halting debug support | Present or absent | Present |
| Multiplier | Fast or small | Fast (single cycle) |
| Single-cycle I/O port | Present or absent | Present |
| Wake-up interrupt controller | Supported or not supported | Not supported |
| Vector Table Offset Register | Present or absent | Present |
| Unprivileged/Privileged support | Present or absent | Absent ⁽¹⁾ |
| Memory Protection Unit | Not present or 8-region | Not present |
| Reset all registers | Present or absent | Absent |
| Instruction fetch width | 16-bit only or mostly 32-bit | 32-bit |

Note:

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

7.1.2. Cortex-M0+ Peripherals

- System Control Space (SCS)
 - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Timer (SysTick)

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

Table 7-4. Bus Matrix Masters

| Bus Matrix Masters | Master ID |
|-----------------------------|-----------|
| CM0+ - Cortex M0+ Processor | 0 |
| DSU - Device Service Unit | 1 |

Table 7-5. Bus Matrix Slaves

| Bus Matrix Slaves | Slave ID |
|-----------------------|----------|
| Internal Flash Memory | 0 |
| AHB-APB Bridge A | 1 |
| AHB-APB Bridge B | 2 |
| AHB-APB Bridge C | 3 |

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBB_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.

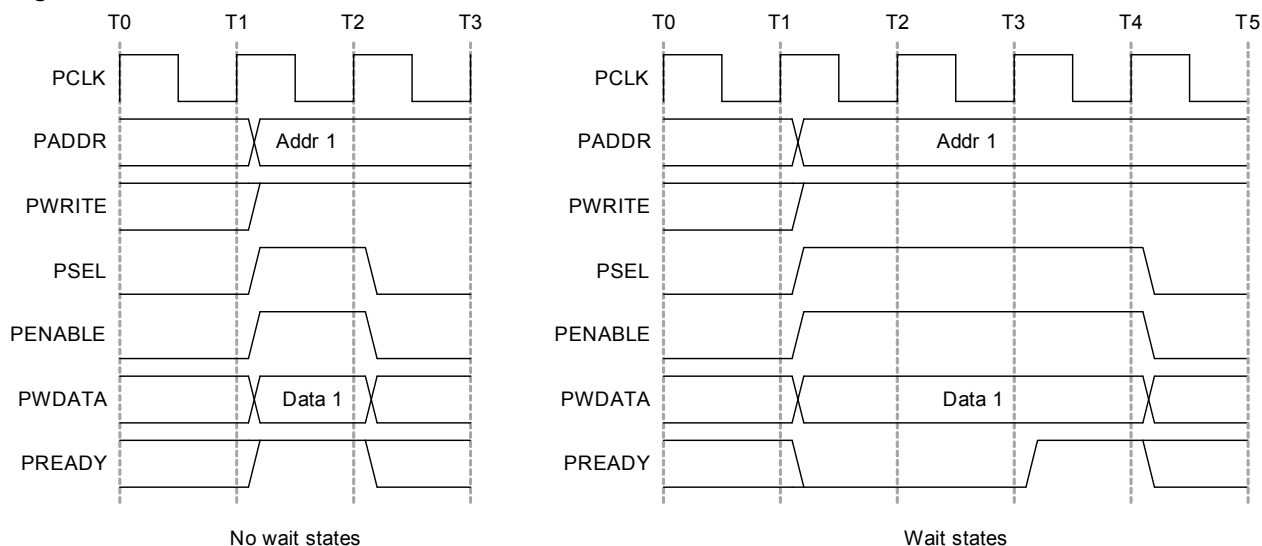
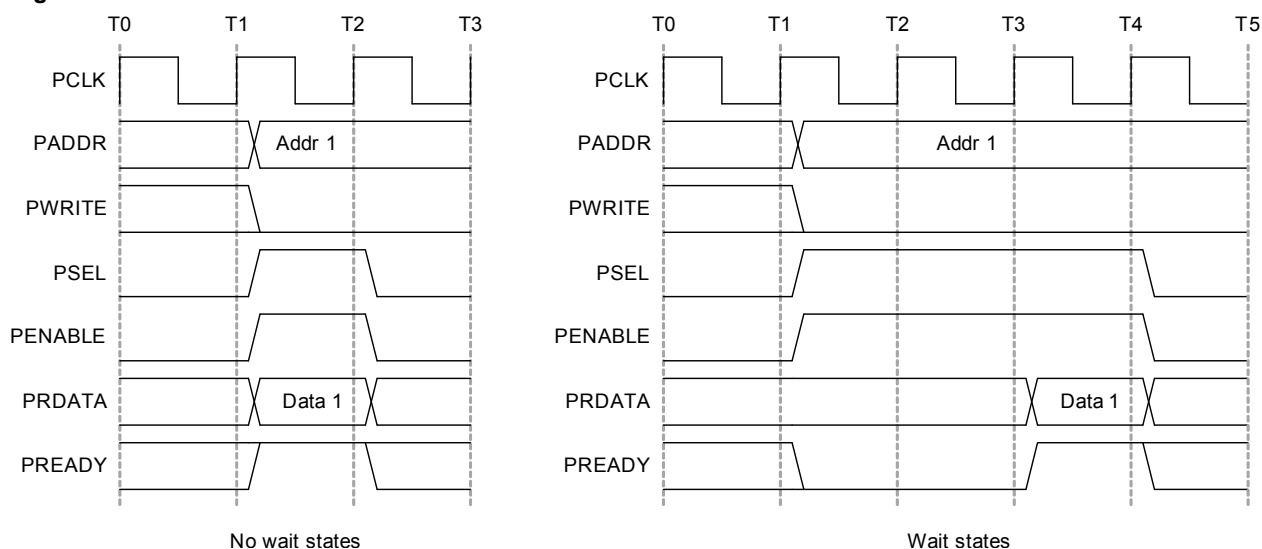


Figure 7-2. APB Read Access.



Related Links

[Product Mapping](#) on page 19

7.6. PAC - Peripheral Access Controller

7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled at reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

7.7.1.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –

| | | | | | | | | |
|--------|----|-----|-----|-----|------|---------|-----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | EIC | RTC | WDT | GCLK | SYSCTRL | PM | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | |

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 4 – WDT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.1.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000000
Property: –

| | | | | | | | | |
|--------|----|-----|-----|-----|------|---------|-----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | EIC | RTC | WDT | GCLK | SYSCTRL | PM | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | |

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 4 – WDT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 1 – PM

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

7.7.2. PAC1 Register Description

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 1 – DSU

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 1 – DSU

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

7.7.3. PAC2 Register Description

Table 8-5. Device and Package Maximum Weight

| | |
|-----|----|
| 200 | mg |
|-----|----|

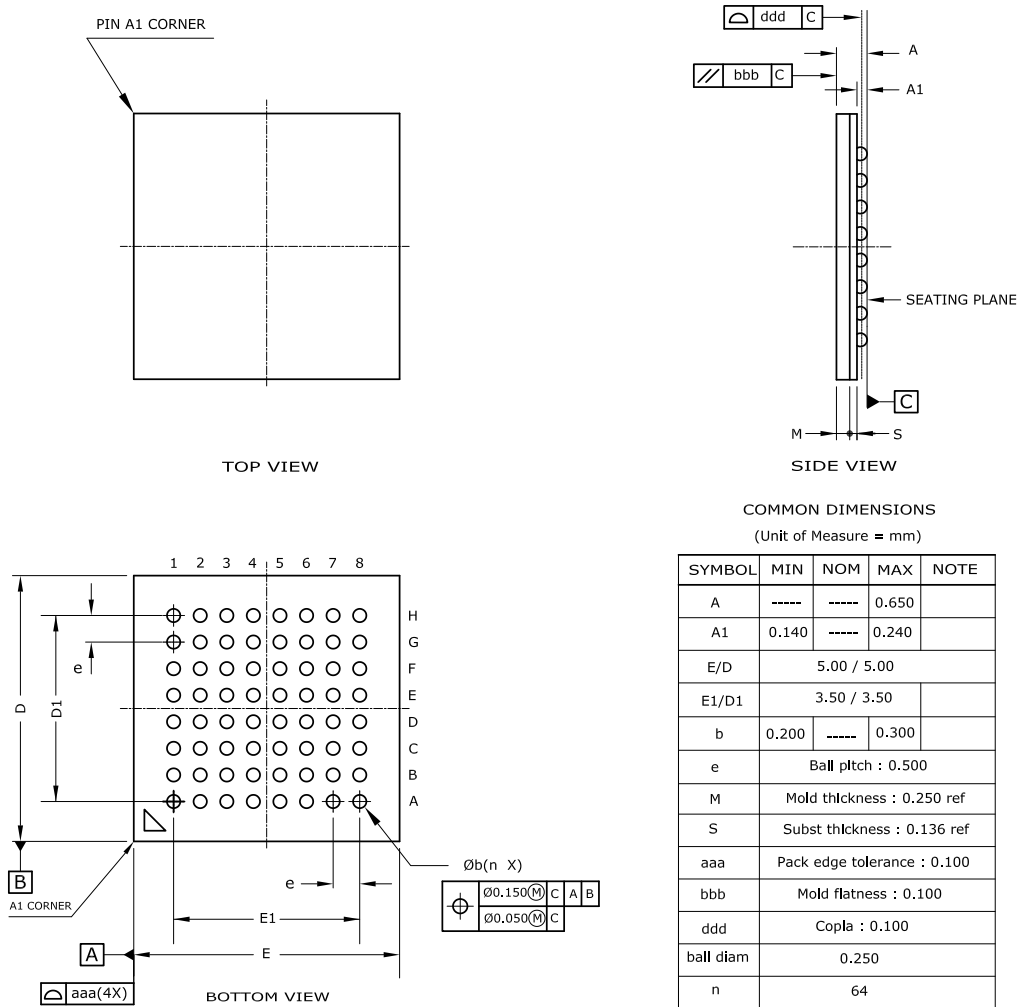
Table 8-6. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

Table 8-7. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

8.2.3. 64-ball UFBGA



- Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
 2. Array as seen from the bottom of the package.
 3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
 4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 8-8. Device and Package Maximum Weight

| | |
|------|----|
| 27.4 | mg |
|------|----|

Table 8-11. Device and Package Maximum Weight

| | |
|-----|----|
| 140 | mg |
|-----|----|

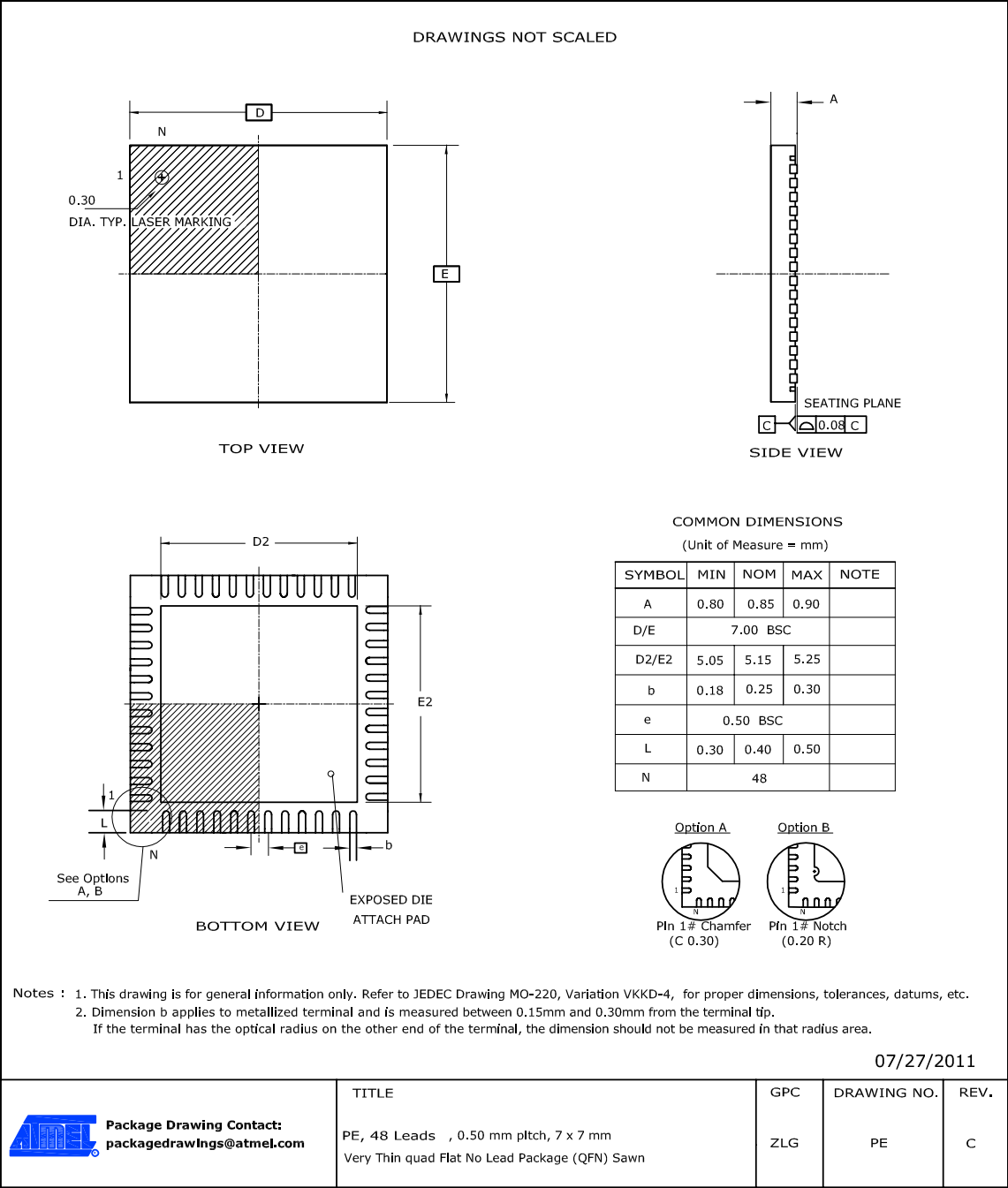
Table 8-12. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

Table 8-13. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

8.2.5. 48 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-14. Device and Package Maximum Weight

| | |
|-----|----|
| 140 | mg |
|-----|----|

Table 8-15. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

Table 8-16. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

8.2.6. 45-ball WLCSP

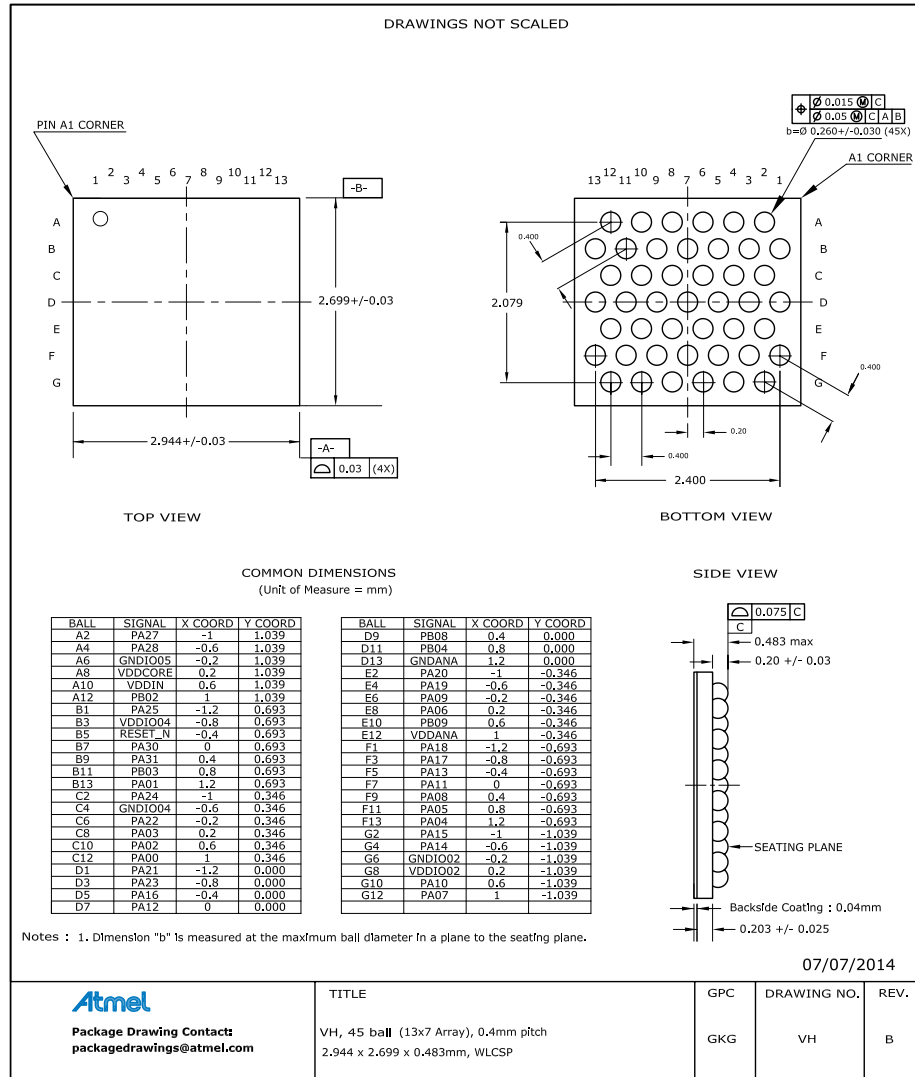


Table 8-17. Device and Package Maximum Weight

| | |
|-----|----|
| 7.3 | mg |
|-----|----|

Table 8-18. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL1 |
|----------------------------|------|

Table 8-19. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E1 |

8.2.7. 32 pin TQFP

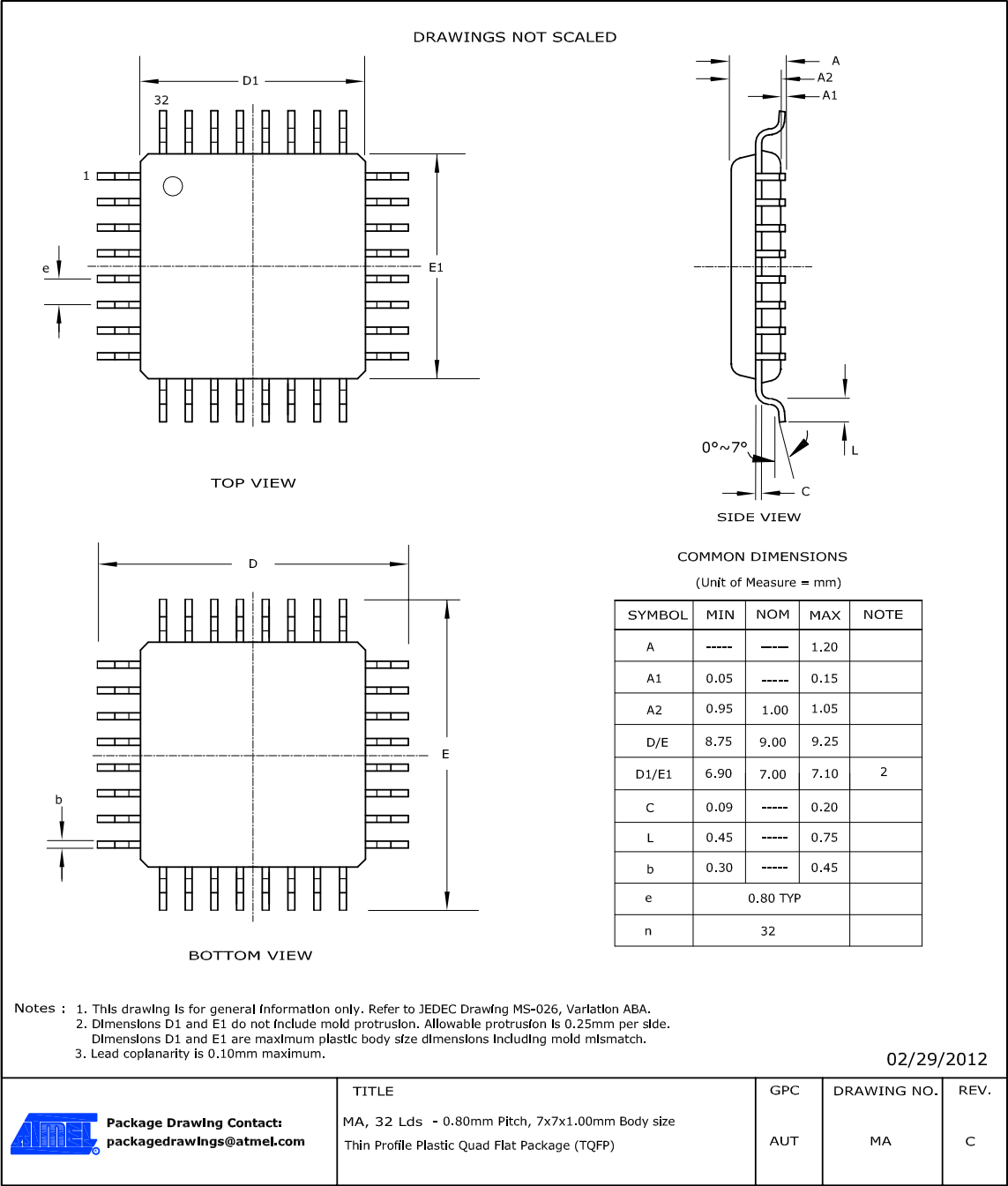


Table 8-20. Device and Package Maximum Weight

| | |
|-----|----|
| 100 | mg |
|-----|----|

Table 8-21. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|