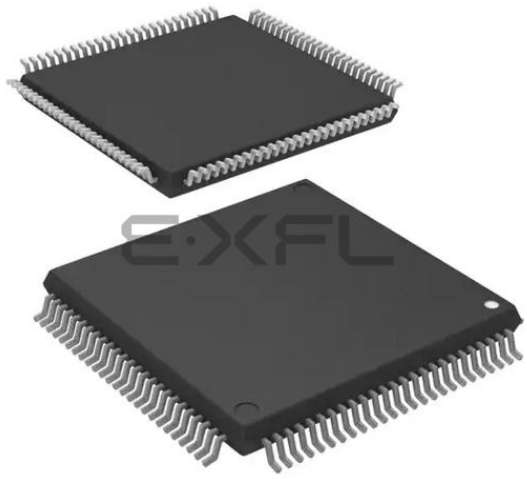
Renesas Electronics America Inc - UPD78F1162AGC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1162agc-ueu-ax

Pin Identification

ANI0 to ANI15: Analog input

ANO0, ANO1: Analog output

ASTB: Address strobe

AV_{REF0}, AV_{REF1}: Analog reference voltage

AV_{SS} : Analog ground

CLKOUT: Clock output

EV_{DD0}, EV_{DD1}: Power supply for port

EV_{SS0}, EV_{SS1}: Ground for port

EX0 to EX31: External extension bus

EXCLK: External clock input (main system clock)

EXLVI: External potential input for low-voltage detector

FLMD0: Flash programming mode

INTP0 to INTP11: External interrupt input

KR0 to KR7: Key return

P00 to P06: Port 0

P10 to P17: Port 1

P20 to P27: Port 2

P30, P31: Port 3

P40 to P47: Port 4

P50 to P57: Port 5

P60 to P67: Port 6

P70 to P77: Port 7

P80 to P87: Port 8

P110, P111: Port 11

P120 to P124: Port 12

P130, P131: Port 13

P140 to P145: Port 14

P150 to P157: Port 15

PCLBUZ0, PCLBUZ1: Programmable clock output/ buzzer output

$\overline{RD}$: Read strobe

REGC: Regulator capacitance

$\overline{RESET}$: Reset

RTC1HZ: Real-time counter correction clock (1 Hz) output

RTCCL: Real-time counter clock (32 kHz original oscillation) output

RTCDIV: Real-time counter clock (32 kHz divided frequency) output

RxD0 to RxD3: Receive data

$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$: Serial clock input/output

SCL0, SCL10, SCL20: Serial clock input/output

SDA0, SDA10, SDA20: Serial data input/output

SI00, SI01, SI10, SI20: Serial data input

SO00, SO01, SO10, SO20: Serial data output

TI00 to TI07: Timer input

TO00 to TO07: Timer output

TOOL0: Data input/output for tool

TOOL1: Clock output for tool

TxD0 to TxD3: Transmit data

V_{DD}: Power supply

V_{SS}: Ground

$\overline{WAIT}$: Wait

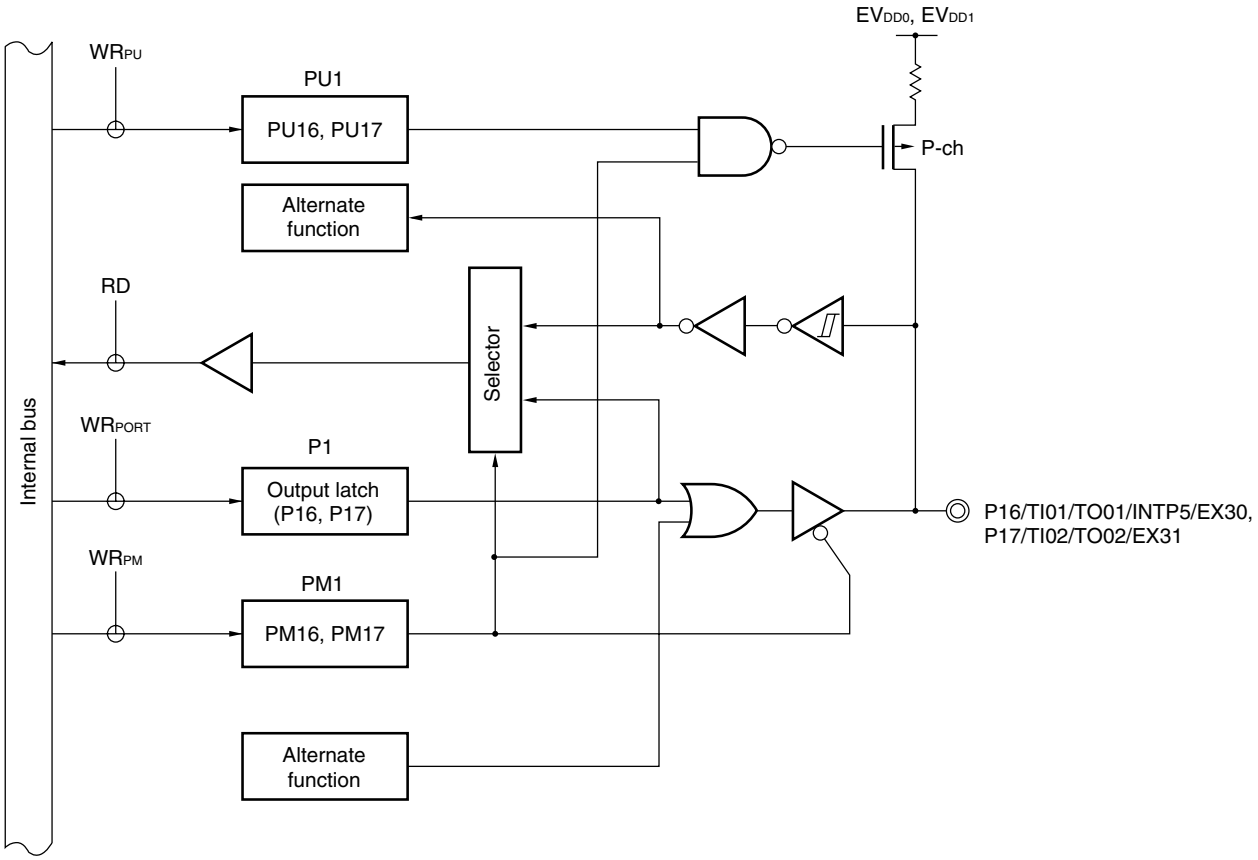
$\overline{WR0}$: Lower byte write strobe

$\overline{WR1}$: Upper byte write strobe

X1, X2: Crystal oscillator (main system clock)

XT1, XT2: Crystal oscillator (subsystem clock)

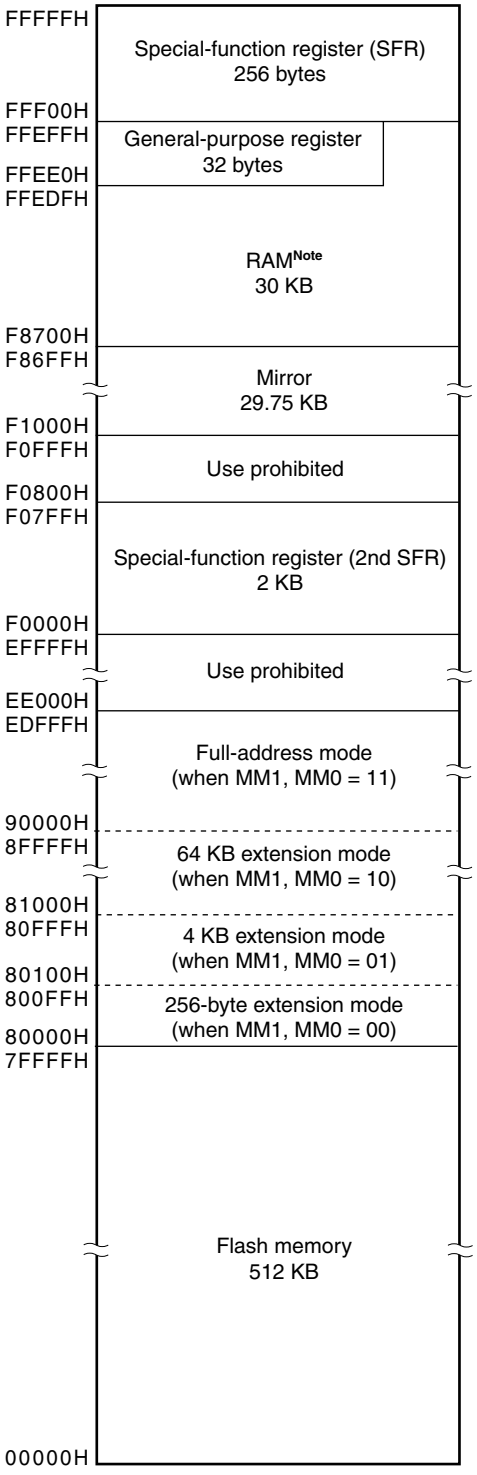
Figure 4-12. Block Diagram of P16 and P17



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 5-1. Memory Map When Using External Bus Interface Function (4/4)

(g) Memory map of μPD78F1168, 78F1168A



Note Use of the area F8700H to F8EFFH is prohibited when using the self-programming function, since this area is used for self-programming library.

Table 6-5. Changing CPU Clock (2/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Subsystem clock[Note]	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1)
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	

Note When changing the subsystem clock to another clock, the clock must be set back to the clock before setting the subsystem clock. For example, when changing the clock to the X1 clock after having changed the internal high-speed oscillation clock to the subsystem clock, the clock is changed in the order of the subsystem clock, the internal high-speed oscillation clock, and the X1 clock.

7.1.2 Functions of each channel when it operates with another channel

Combination operation functions are those functions that are attained by using the master channel (mostly the reference timer that controls cycles) and the slave channels (timers that operate following the master channel) in combination (for details, refer to **7.6.1 Overview of single-operation function and combination operation function**).

(1) PWM (Pulse Width Modulator) output

Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.

(2) One-shot pulse output

Two channels are used as a set to generate a one-shot pulse with a specified delay time and a specified pulse width.

(3) Multiple PWM (Pulse Width Modulator) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.

7.1.3 LIN-bus supporting function (channel 7 only)

(1) Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD3) of UART3 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

(2) Detection of sync break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD3) of UART3 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a sync break field.

(3) Measurement of pulse width of sync field

After a sync break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD3) of UART3 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

Figure 8-4. Format of Real-Time Counter Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time counter
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of RWAIT is valid. Before reading or writing the counter value, confirm that the value of this flag is 1. Table 8-2 shows the displayed time digits.	

RWAIT	Wait control of real-time counter
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. Because RSUBC continues operation, complete reading or writing of it in 1 second, and clear this bit back to 0. When RWAIT = 1, it takes up to 1 clock (32.768 kHz) until the counter value can be read or written. If RSUBC overflows when RWAIT = 1, it counts up after RWAIT = 0. If the second count register is written, however, it does not count up because RSUBC is cleared.	

Caution The RIFG and WAFG flags may be cleared when the RTCC1 register is written by using a 1-bit manipulation instruction. Use, therefore, an 8-bit manipulation instruction in order to write to the RTCC1 register. To prevent the RIFG and WAFG flags from being cleared during writing, disable writing by setting “1” to the corresponding bit. When the value may be rewritten because the RIFG and WAFG flags are not being used, the RTCC1 register may be written by using a 1-bit manipulation instruction.

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

9.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

(1) Watchdog timer enable register (WDTE)

Writing “ACH” to WDTE clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH[Note].

Figure 9-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FFFABH After reset: 9AH/1AH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE reset value differs depending on the WDTON setting value of the option byte (000C0H). To operate watchdog timer, set WDTON to 1.

WDTON Setting Value	WDTE Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Cautions 1. If a value other than “ACH” is written to WDTE, an internal reset signal is generated.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.

3. The value read from WDTE is 9AH/1AH (this differs from the written value (ACH)).

13.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20) Communication

This is a clocked communication function that uses three lines: serial clock ($\overline{SCK}$) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

The channels supporting 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20) are channels 0 to 2 of SAU0 and channel 0 of SAU1.

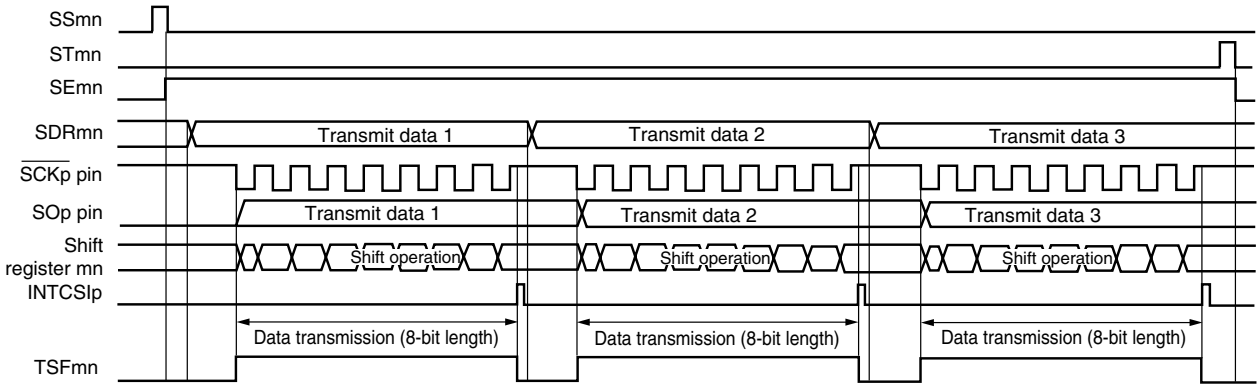
Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

3-wire serial I/O (CSI00, CSI01, CIS10, CSI20) performs the following six types of communication operations.

- Master transmission (See **13.5.1**.)
- Master reception (See **13.5.2**.)
- Master transmission/reception (See **13.5.3**.)
- Slave transmission (See **13.5.4**.)
- Slave reception (See **13.5.5**.)
- Slave transmission/reception (See **13.5.6**.)

(3) Processing flow (in single-transmission mode)

Figure 13-52. Timing Chart of Slave Transmission (in Single-Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)

13.5.7 Calculating transfer clock frequency

The transfer clock frequency for 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20) communication can be calculated by the following expressions.

(1) Master

(Transfer clock frequency) = {Operation clock (MCK) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [Hz]

(2) Slave

(Transfer clock frequency) = {Frequency of serial clock ($\overline{SCK}$) supplied by master}[Note] [Hz]

Note The permissible maximum transfer clock frequency is f_{MCK}/6.

Remarks 1. The value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000000B to 1111111B) and therefore is 0 to 127.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

The operation clock (MCK) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

(1) Register setting

Figure 13-97. Example of Contents of Registers for Data Transmission of Simplified I^2C (IIC10, IIC20)

(a) Serial output register m (SOm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2 0/1Note	CKOm1 ×	CKOm0 0/1Note	0	0	0	0	1	SOm2 0/1Note	SOm1 ×	SOm0 0/1Note

(b) Serial output enable register m (SOEm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1	SOEm1 ×	SOEm0 0/1

(c) Serial channel start register m (SSm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1	SSm1 ×	SSm0 0/1

(d) Serial mode register mn (SMRmn) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn 0/1	CCSmn 0	0	0	0	0	0	STSmn 0	0	SISmn0 0	1	0	0	MDmn2 1	MDmn1 0	MDmn0 0

(e) Serial communication operation setting register mn (SCRmn) … Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn 1	RXEmn 0	DAPmn 0	CKPmn 0	0	EOCmn 0	PTCmn1 0	PTCmn0 0	DIRmn 0	0	SLCmn1 0	SLCmn0 1	0	DLSmn2 1	DLSmn1 1	DLSmn0 1

(f) Serial data register mn (SDRmn) (lower 8 bits: SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting							0	Transmit data setting							

SIOr

Note The value varies depending on the communication data during communication operation.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
□: Setting is fixed in the IIC mode, ▢: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

24.4 Setting of Option Byte

The user option byte and on-chip debug option byte can be set using the RA78K0R or PM+ linker option, in addition to describing to the source. When doing so, the contents set by using the linker option take precedence, even if descriptions exist in the source, as mentioned below.

See the **RA78K0R Assembler Package User's Manual** for how to set the linker option.

A software description example of the option byte setting is shown below.

```
OPT   CSEG       OPT_BYTE
      DB         10H     ; Does not use interval interrupt of watchdog timer,
                         ; Enables watchdog timer operation,
                         ; Window open period of watchdog timer is 25%,
                         ; Overflow time of watchdog timer is 2^10/fIL,
                         ; Stops watchdog timer operation during HALT/STOP mode
      DB         0FFH    ; Stops LVI default start function
      DB         0FFH    ; Reserved area
      DB         85H     ; Enables on-chip debug operation, does not erase flash memory
                         ; data when security ID authorization fails
```

When the boot swap function is used during self programming, 000C0H to 000C3H is switched to 010C0H to 010C3H. Describe to 010C0H to 010C3H, therefore, the same values as 000C0H to 000C3H as follows.

```
OPT2  CSEG   AT   010C0H
      DB         10H     ; Does not use interval interrupt of watchdog timer,
                         ; Enables watchdog timer operation,
                         ; Window open period of watchdog timer is 25%,
                         ; Overflow time of watchdog timer is 2^10/fIL,
                         ; Stops watchdog timer operation during HALT/STOP mode
      DB         0FFH    ; Stops LVI default start function
      DB         0FFH    ; Reserved area
      DB         85H     ; Enables on-chip debug operation, does not erase flash memory
                         ; data when security ID authorization fails
```

Caution To specify the option byte by using assembly language, use OPT_BYTE as the relocation attribute name of the CSEG pseudo instruction. To specify the option byte to 010C0H to 010C3H in order to use the boot swap function, use the relocation attribute AT to specify an absolute address.

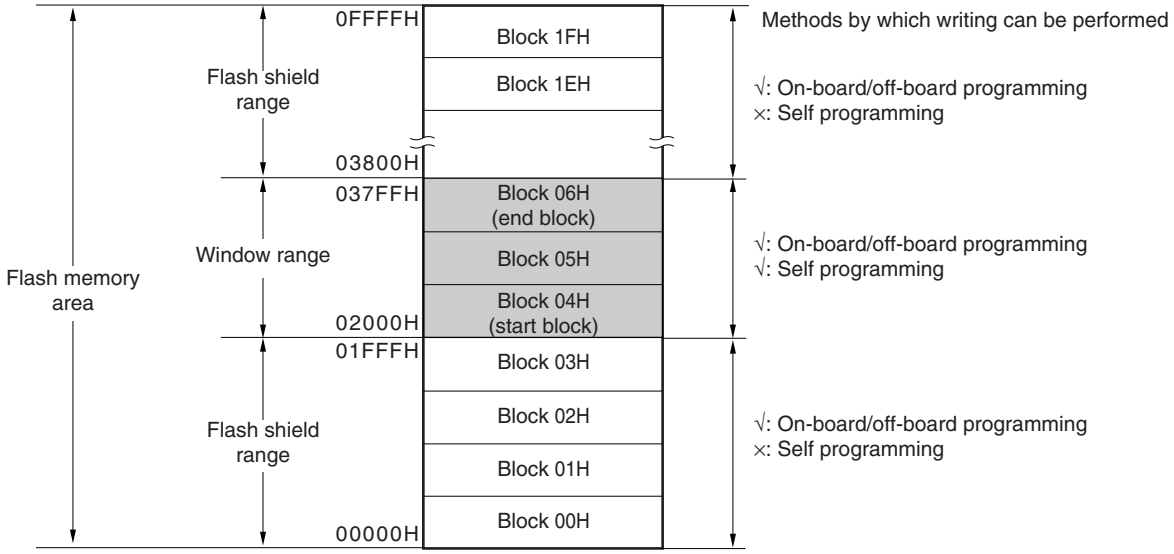
25.9.2 Flash shield window function

The flash shield window function is provided as one of the security functions for self programming. It disables writing to and erasing areas outside the range specified as a window only during self programming.

The window range can be set by specifying the start and end blocks. The window range can be set or changed during both on-board/off-board programming and self programming.

Writing to and erasing areas outside the window range are disabled during self programming. During on-board/off-board programming, however, areas outside the range specified as a window can be written and erased.

Figure 25-14. Flash Shield Window Setting Example
(Target Devices: μPD78F1162, 78F1162A, Start Block: 04H, End Block: 06H)



Caution If the rewrite-prohibited area of the boot cluster 0 overlaps with the flash shield window range, prohibition to rewrite the boot cluster 0 takes priority.

Table 25-11. Relationship Between Flash Shield Window Function Setting/Change Methods and Commands

Programming Conditions	Window Range Setting/Change Methods	Execution Commands	
		Block Erase	Write
Self-programming	Specify the starting and ending blocks by the set information library.	Block erasing is enabled only within the window range.	Writing is enabled only within the range of window range.
On-board/off-board programming	Specify the starting and ending blocks on GUI of dedicated flash memory programmer, etc.	Block erasing is enabled also outside the window range.	Writing is enabled also outside the window range.

Remark See **25.7 Security Settings** to prohibit writing/erasing during on-board/off-board programming.

28.1 Conventions Used in Operation List

28.1.1 Operand identifiers and specification methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, !!, $, $!, [ ], and ES: are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: 16-bit absolute address specification
- !!: 20-bit absolute address specification
- $: 8-bit relative address specification
- $!: 16-bit relative address specification
- [ ]: Indirect address specification
- ES:: Extension address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, !!, $, $!, [ ], and ES: symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 28-1. Operand Identifiers and Specification Methods

Identifier	Description Method
r rp sfr sfrp	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special-function register symbol (SFR symbol) FFF00H to FFFFFH Special-function register symbols (16-bit manipulatable SFR symbol. Even addresses only[Note]) FFF00H to FFFFFH
saddr saddrp	FFE20H to FFF1FH Immediate data or labels FFE20H to FFF1FH Immediate data or labels (even addresses only[Note])
addr20 addr16 addr5	00000H to FFFFFH Immediate data or labels 0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions[Note]) 0080H to 00BFH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label
RBn	RB0 to RB3

Note Bit 0 = 0 when an odd address is specified.

Remark The special function registers can be described to operand sfr as symbols. See **Table 3-5 SFR List** for the symbols of the special function registers.

The extended special function registers can be described to operand !addr16 as symbols. See **Table 3-6 Extended SFR (2nd SFR) List** for the symbols of the extended special function registers.

DC Characteristics (16/16)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	V_{DD} = 3.0 V		0.2	1.0	μA
			V_{DD} = 2.0 V		0.2	1.0	
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 240 kHz			5	10	μA
A/D converter operating current	I_{ADC} Note 4	During conversion at maximum speed, 2.3 V ≤ AV_{REF0}			0.86	1.9	mA
D/A converter operating current	I_{DAC} Note 5	Per 1 channel			1.0	2.5	mA
LVI operating current	I_{LVI} Note 6				9	18	μA

Notes 1. Current flowing only to the real-time counter (excluding the operating current of the XT1 oscillator). The current value of the 78K0R/KG3 is the TYP. value, the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time counter operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time counter operating current.

2. When internal high-speed oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the 78K0R/KG3 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB}/2 or when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter (AV_{REF0} pin). The current value of the 78K0R/KG3 is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the D/A converter (AV_{REF1} pin). The current value of the 78K0R/KG3 is the sum of I_{DD1} or I_{DD2} and I_{DAC} when the D/A converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVI circuit. The current value of the 78K0R/KG3 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the operation mode, HALT or STOP mode.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency
f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
f_{CLK}: CPU/peripheral hardware clock frequency

<R> **2.** Temperature condition of the TYP. value is T_A = 25°C

- **Expanded-specification products (μPD78F116xA)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle	t_{CYK}	<1>	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
			1.8 V ≤ V_{DD} < 2.7 V	200			ns
CLKOUT high-level width	t_{WKH}	<2>	2.7 V ≤ V_{DD} ≤ 5.5 V	0.4t_{CYK} – 30		0.6t_{CYK}	ns
			1.8 V ≤ V_{DD} < 2.7 V	0.4t_{CYK} – 50		0.6t_{CYK}	ns
CLKOUT low-level width	t_{WKL}	<3>	2.7 V ≤ V_{DD} ≤ 5.5 V	0.4t_{CYK} – 30		0.6t_{CYK}	ns
			1.8 V ≤ V_{DD} < 2.7 V	0.4t_{CYK} – 50		0.6t_{CYK}	ns
ASTB high-level width	t_{WASH1}	<4>	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8t_{CYK} – 40		1.2t_{CYK}	ns
			1.8 V ≤ V_{DD} < 2.7 V	0.8t_{CYK} – 60		1.2t_{CYK}	ns
$\overline{RD}$ low-level width	t_{WRDL1}	<5>	2.7 V ≤ V_{DD} ≤ 5.5 V	(0.8 + m + w) t_{CYK} – 40		(1.2 + m + w) t_{CYK}	ns
			1.8 V ≤ V_{DD} < 2.7 V	(0.8 + m + w) t_{CYK} – 60		(1.2 + m + w) t_{CYK}	ns
$\overline{WR0}$, $\overline{WR1}$ low-level width	t_{WWRL1}	<6>	2.7 V ≤ V_{DD} ≤ 5.5 V	(0.8 + w) t_{CYK} – 40		(1.2 + w) t_{CYK}	ns
			1.8 V ≤ V_{DD} < 2.7 V	(0.8 + w) t_{CYK} – 60		(1.2 + w) t_{CYK}	ns
Delay time from CLKOUT↑ to ASTB	t_{DKAS1}	<7>	2.7 V ≤ V_{DD} ≤ 5.5 V	2		50	ns
			1.8 V ≤ V_{DD} < 2.7 V	2		80	ns
Delay time from CLKOUT↑ to $\overline{RD}$	t_{DKRD1}	<8>	2.7 V ≤ V_{DD} ≤ 5.5 V	2		50	ns
			1.8 V ≤ V_{DD} < 2.7 V	2		80	ns
Delay time from CLKOUT↑ to $\overline{WR0}$, $\overline{WR1}$	t_{DKWR1}	<9>	2.7 V ≤ V_{DD} ≤ 5.5 V	2		50	ns
			1.8 V ≤ V_{DD} < 2.7 V	2		80	ns
Delay time from CLKOUT↑ to address	t_{DKA1}	<10>	2.7 V ≤ V_{DD} ≤ 5.5 V	2		55	ns
			1.8 V ≤ V_{DD} < 2.7 V	2		90	ns
Data output delay time from CLKOUT↑	t_{DKOD1}	<11>	2.7 V ≤ V_{DD} ≤ 5.5 V	2		55	ns
			1.8 V ≤ V_{DD} < 2.7 V	2		90	ns
Data output hold time from CLKOUT↑	t_{HKOD1}	<12>	2.7 V ≤ V_{DD} ≤ 5.5 V	2			ns
			1.8 V ≤ V_{DD} < 2.7 V	2			ns
Data input setup time to CLKOUT↑	t_{SKDI1}	<13>	2.7 V ≤ V_{DD} ≤ 5.5 V	40			ns
			1.8 V ≤ V_{DD} < 2.7 V	85			ns
Data input hold time from CLKOUT↑	t_{HKDI1}	<14>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
			1.8 V ≤ V_{DD} < 2.7 V	0			ns
$\overline{WAIT}$ setup time to CLKOUT↑	t_{SKWT1}	<15>	2.7 V ≤ V_{DD} ≤ 5.5 V	45			ns
			1.8 V ≤ V_{DD} < 2.7 V	85			ns
$\overline{WAIT}$ hold time from CLKOUT↑	t_{HKWT1}	<16>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
			1.8 V ≤ V_{DD} < 2.7 V	0			ns
Delay time from address output stop to $\overline{RD}$↓	t_{DAR1}	<17>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
			1.8 V ≤ V_{DD} < 2.7 V	0			ns

Remarks 1. C_L: The pin load capacitance is 15 pF.

2. Test points: V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

3. m = 0: Multiplexed bus mode

m = 1: Separate bus mode

w: Number of waits with $\overline{WAIT}$

Recommended Oscillator Constants

(1) X1 oscillation: Ceramic resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd.	CSTCC2M00G56-R0	SMD	2.0	Internal (47)	Internal (47)	1.8	5.5
	CSTCR4M00G55-R0	SMD	4.0	Internal (39)	Internal (39)	1.8	
	CSTLS4M00G56-B0	Lead		Internal (47)	Internal (47)	1.8	
	CSTCR4M19G55-R0	SMD	4.194	Internal (39)	Internal (39)	1.8	
	CSTLS4M19G56-B0	Lead		Internal (47)	Internal (47)	1.8	
	CSTCR4M91G55-R0	SMD	4.915	Internal (39)	Internal (39)	1.8	
	CSTLS4M91G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS4M91G56-B0			Internal (47)	Internal (47)	2.1	
	CSTCR5M00G53-R0	SMD	5.0	Internal (15)	Internal (15)	1.8	
	CSTCR5M00G55-R0			Internal (39)	Internal (39)	1.8	
	CSTLS5M00G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS5M00G56-B0			Internal (47)	Internal (47)	2.1	
	CSTCR6M00G53-R0	SMD	6.0	Internal (15)	Internal (15)	1.8	
	CSTCR6M00G55-R0			Internal (39)	Internal (39)	1.9	
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS6M00G56-B0			Internal (47)	Internal (47)	2.2	
	CSTCE8M00G52-R0	SMD	8.0	Internal (10)	Internal (10)	1.8	
	CSTCE8M00G55-R0			Internal (33)	Internal (33)	1.9	
	CSTLS8M00G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS8M00G56-B0			Internal (47)	Internal (47)	2.4	
	CSTCE8M38G52-R0	SMD	8.388	Internal (10)	Internal (10)	1.8	
	CSTCE8M38G55-R0			Internal (33)	Internal (33)	1.9	
	CSTLS8M38G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS8M38G56-B0			Internal (47)	Internal (47)	2.4	
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	1.8	
	CSTCE10M0G55-R0			Internal (33)	Internal (33)	2.1	
	CSTLS10M0G53-B0	Lead		Internal (15)	Internal (15)	1.8	
TOKO, Inc.	DCRHTC(P)2.00LL	Lead	2.0	Internal (30)	Internal (30)	1.8	5.5
	DCRHTC(P)4.00LL		4.0	Internal (30)	Internal (30)		
	DECRHTC4.00	SMD	4.0	Internal (15)	Internal (15)		
	DCRHYC(P)8.00A	Lead	8.0	Internal (22)	Internal (22)		

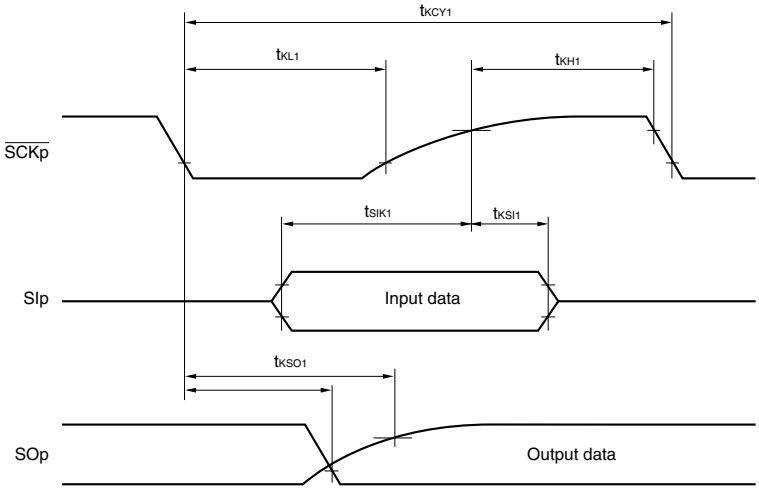
Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.**

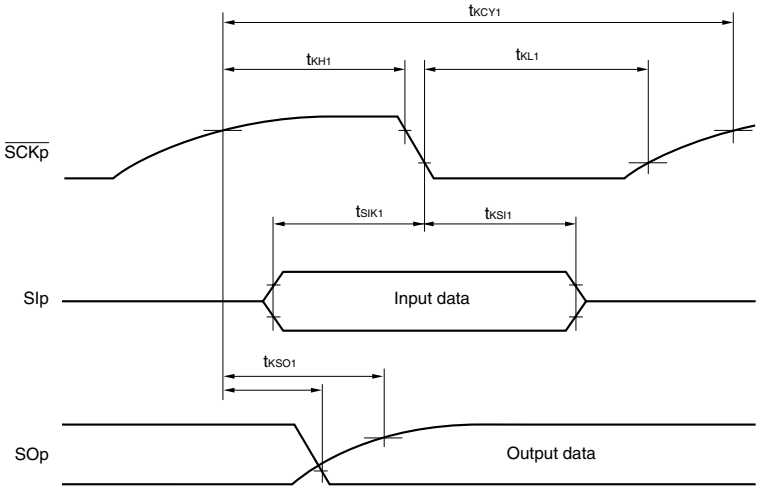
The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KG3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(3) Serial interface: Serial array unit (13/18)

CSI mode serial transfer timing (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Caution Select the TTL input buffer for SIp and the N-ch open-drain output (V_{DD} tolerance) mode for SOp and $\overline{\text{SCKp}}$ by using the PIMg and POMg registers.

Remarks 1. p: CSI number (p = 01, 10, 20), g: PIM and POM number (g = 0, 4, 14)

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

3. CSI00 cannot communicate at different potential. Use CSI01, CSI10, and CSI20 for communication at different potential.

(5) Serial interface: On-chip debug (UART)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

(a) On-chip debug (UART)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			$f_{CLK}/2^{12}$		$f_{CLK}/6$	bps
		Flash memory programming mode			2.66	Mbps
TOOL1 output frequency	f_{TOOL1}	2.7 V ≤ V_{DD} ≤ 5.5 V			10	MHz
		1.8 V ≤ V_{DD} < 2.7 V			2.5	MHz

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 13	Soft	Registers controlling serial array unit	SOEm: Serial output enable register m	Be sure to clear bits 15 to 3 of SOE0, and bits 15 to 3 and 1 of SOE1 to “0”.	p.411 ☐
			SOm: Serial output register m	Be sure to set bits 11 and 3 of SO0, and bits 11 to 9, 3, and 1 of SO1 to “1”. And be sure to clear bits 15 to 12 and 7 to 4 of SOm to “0”.	p.412 ☐
			SOLm: Serial output level register m	Be sure to clear bits 15 to 3 and 1 to “0”.	p.413 ☐
			ISC: Input switch control register	Be sure to clear bits 7 to 2 to “0”.	p.414 ☐
			NFEN0: Noise filter enable register 0	Be sure to clear bits 7, 5, 3, and 1 to “0”.	p.415 ☐
		Operation stop mode	Stopping the operation by units	If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for input switch control register (ISC), noise filter enable register (NFEN0), port input mode registers (PIM0, PIM4, PIM14), port output mode registers (POM0, POM4, POM14), port mode registers (PM0, PM1, PM4, PM14), and port registers (P0, P1, P4, P14)).	p.418 ☐
				Be sure to clear bit 1 of the PER0 register to 0.	p.418 ☐
		3-wire serial I/O (CSI00, CSI01, CSI10, CSI20) communication	Master transmission	After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	pp.424, 428, 430 ☐
			Master transmission (in continuous transmission mode)	The MDmn0 bit can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.	p.429 ☐
			Master reception	After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	pp.433, 436, 438 ☐
			Master reception (in continuous reception mode)	The MDmn0 bit can be rewritten even during operation. However, rewrite it before receive of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last receive data.	p.437 ☐
			Master transmission/ reception	After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	pp.441, 444, 446 ☐
			Master transmission/ reception (in continuous transmission/ reception mode)	The MDmn0 bit can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.	p.445 ☐
			Slave transmission	After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.	pp.449, 453, 455 ☐
			Slave transmission (in continuous transmission mode)	The MDmn0 bit can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.	p.454 ☐