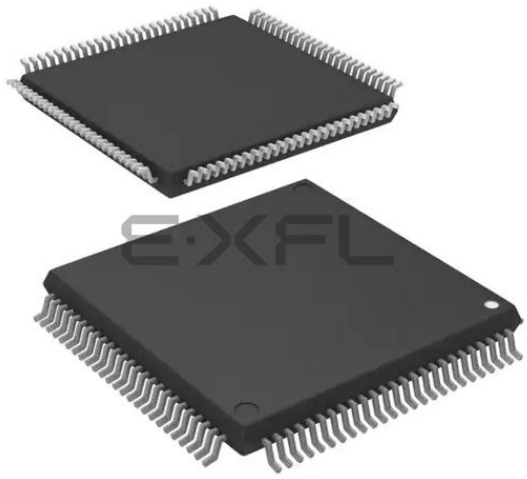
Renesas Electronics America Inc - UPD78F1162AGF-GAS-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1162agf-gas-ax

RENESAS

User's Manual

78K0R/KG3

16-bit Single-Chip Microcontrollers

μPD78F1162, 78F1162A, 78F1162A(A)
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μPD78F1166, 78F1166A, 78F1166A(A)
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Document No. U17894EJ9V0UD00 (9th edition)
Date Published July 2009 NS

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Figure 6-5. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFFA3H After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				fx = 10 MHz	fx = 20 MHz
0	0	0	2^8/fx	25.6 μs	Setting prohibited
0	0	1	2^9/fx	51.2 μs	25.6 μs
0	1	0	2^{10}/fx	102.4 μs	51.2 μs
0	1	1	2^{11}/fx	204.8 μs	102.4 μs
1	0	0	2^{13}/fx	819.2 μs	409.6 μs
1	0	1	2^{15}/fx	3.27 ms	1.64 ms
1	1	0	2^{17}/fx	13.11 ms	6.55 ms
1	1	1	2^{18}/fx	26.21 ms	13.11 ms

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.

2. Setting the oscillation stabilization time to 20 μs or less is prohibited.

3. To change the setting of the OSTS register, be sure to confirm that the counting operation of the OSTC register has been completed.

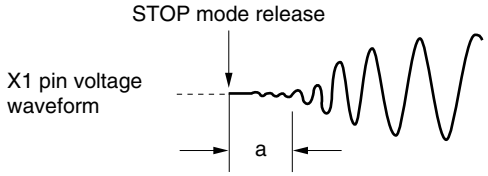
4. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

5. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS.

In the following cases, set the oscillation stabilization time of OSTS to the value greater than or equal to the count value which is to be checked by the OSTC register.

- **If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after the STOP mode is released.**)

6. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark fx: X1 clock oscillation frequency

Figure 13-1 shows the block diagram of serial array unit 0.

Figure 13-1. Block Diagram of Serial Array Unit 0

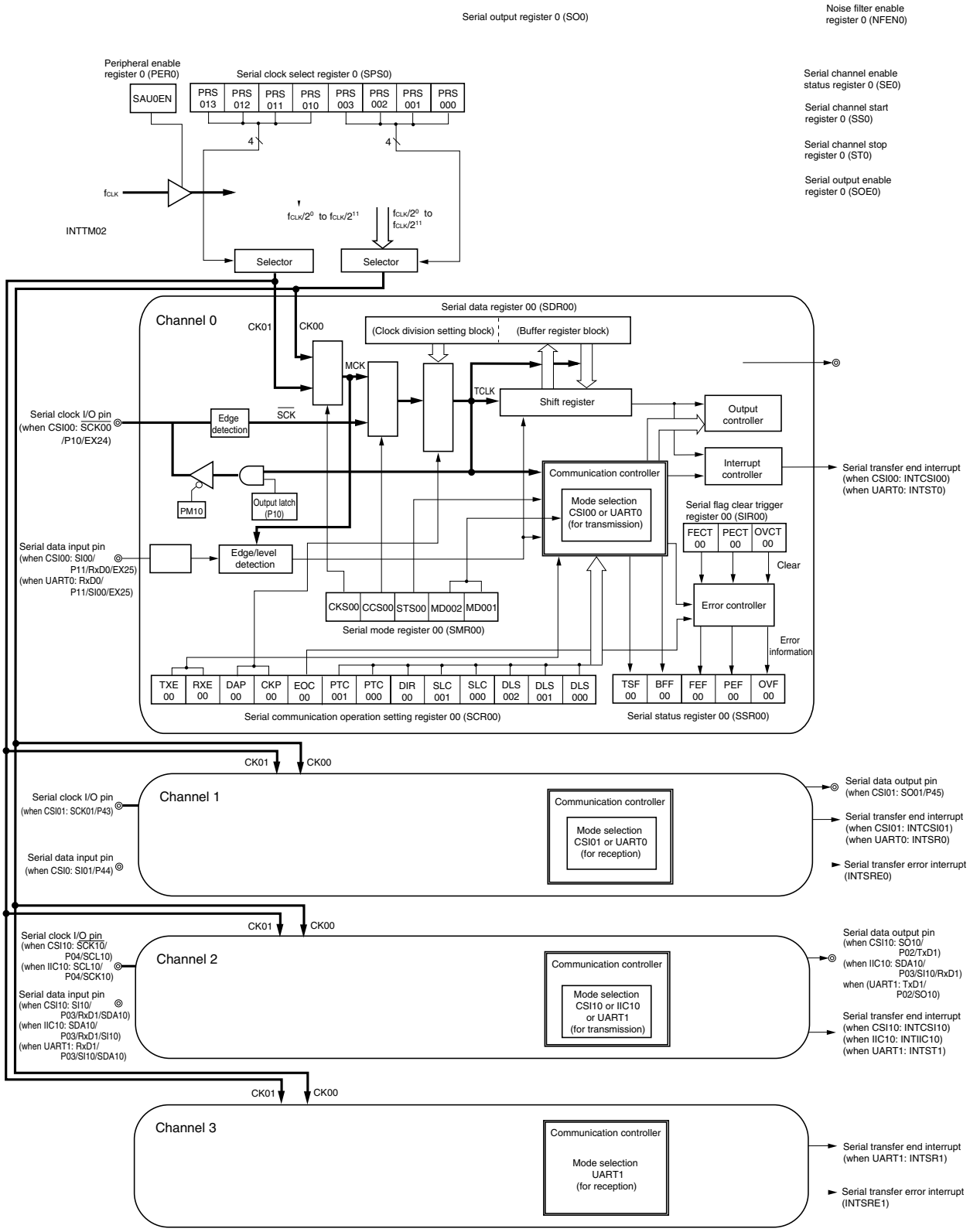
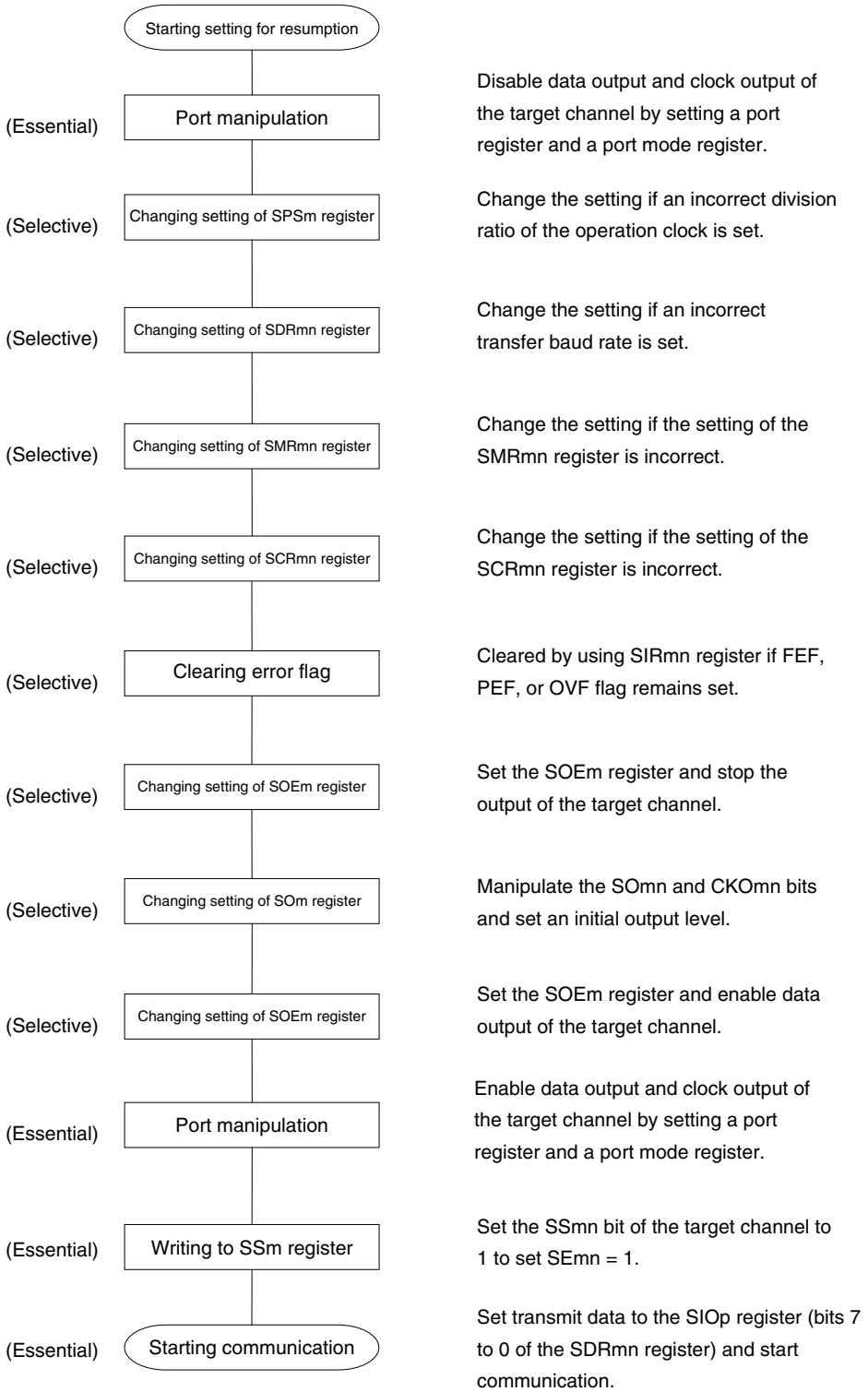
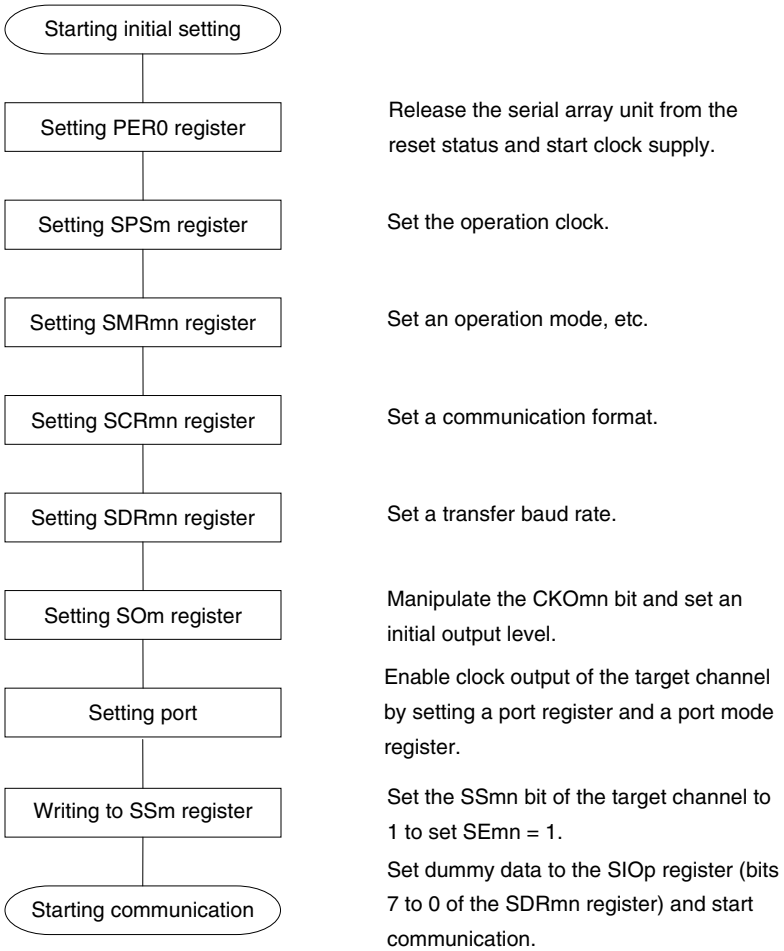


Figure 13-27. Procedure for Resuming Master Transmission



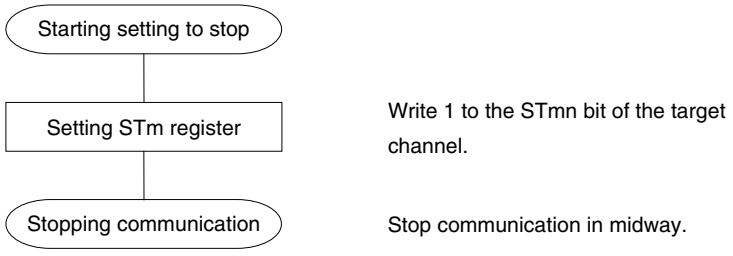
(2) Operation procedure

Figure 13-33. Initial Setting Procedure for Master Reception



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Figure 13-34. Procedure for Stopping Master Reception



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set the SOm register (see **Figure 13-35 Procedure for Resuming Master Reception**).

(1) Register setting

Figure 13-56. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20)

(a) Serial output register m (SOm) …The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2 ×	CKOm1 ×	CKOm0 ×	0	0	0	0	1	SOm2 ×	SOm1 ×	SOm0 ×

<R> **(b) Serial output enable register m (SOEm) …The register that not used in this mode.**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 ×	SOEm1 ×	SOEm0 ×

(c) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1	SSm1 0/1	SSm0 0/1

(d) Serial mode register mn (SMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn 0/1	CCSmn 1	0	0	0	0	0	STSmn 0	0	SISmn0 0	1	0	0	MDmn2 0	MDmn1 0	MDmn0 0

Interrupt sources of channel n
0: Transfer end interrupt

(e) Serial communication operation setting register mn (SCRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn 0	RXEmn 1	DAPmn 0/1	CKPmn 0/1	0	EOCmn 0	PTCmn1 0	PTCmn0 0	DIRmn 0/1	0	SLCmn1 0	SLCmn0 0	0	DLSmn2 1	DLSmn1 1	DLSmn0 0/1

(f) Serial data register mn (SDRmn) (lower 8 bits: SIOp)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	0000000 (baud rate setting)							0	Receive data register							

SIOp

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)
□: Setting is fixed in the CSI slave reception mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

13.7 Operation of Simplified I ^{2}C (IIC10, IIC20) Communication

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This communication function is designed to execute single communication with devices such as EEPROM, flash memory, and A/D converter, and therefore, can be used only by the master and does not have a wait detection function. Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function[Note] and ACK detection function
- Data length of 8 bits
  (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

<R>
- Overrun error
- Parity error (ACK error)

* [Functions not supported by simplified I^{2}C]
  - Slave transmission, slave reception
  - Arbitration loss detection function
  - Wait detection function

Note An ACK is not output when the last data is being received by writing 0 to the SOEmn (SOEm register) bit and stopping the output of serial communication data. See 13.7.3 (2) Processing flow for details.

Remarks 1. To use the full-function I^{2}C bus, see CHAPTER 14 SERIAL INTERFACE IIC0 .
2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

The channels supporting simplified I^{2}C (IIC10, IIC20) are channel 2 of SAU0 and channel 0 of SAU1.

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^{2}C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

Simplified I^{2}C (IIC10, IIC20) performs the following four types of communication operations.

- Address field transmission (See 13.7.1.)
- Data transmission (See 13.7.2.)
- Data reception (See 13.7.3.)
- Stop condition generation (See 13.7.4.)

Figure 14-6. Format of IIC Control Register 0 (IICC0) (3/4)

<R>

STT0[Note]	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in standby state, when IICBSY = 0): Generate a start condition (for starting as master). When the SCL0 line is high level, the SDA0 line is changed from high level to low level and then the start condition is generated. Next, after the rated amount of time has elapsed, SCL0 is changed to low level (wait state). When a third party is communicating: • When communication reservation function is enabled (IICRSV = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSV = 1) STCF is set to 1 and STT0 is cleared. No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.

Cautions concerning set timing

- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when ACKE0 has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A start condition cannot be generated normally during the acknowledge period. Set to 1 during the wait period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as SPT0.
- Setting STT0 to 1 and then setting it again before it is cleared to 0 is prohibited.

Condition for clearing (STT0 = 0)	Condition for setting (STT0 = 1)
• Cleared by setting SST0 to 1 while communication reservation is prohibited. • Cleared by loss in arbitration • Cleared after start condition is generated by master device • Cleared by LREL0 = 1 (exit from communications) • When IICE0 = 0 (operation stop) • Reset	• Set by instruction

Note The signal of this bit is invalid while IICE0 is 0.

Remarks 1. Bit 1 (STT0) becomes 0 when it is read after data setting.

2. IICRSV: Bit 0 of IIC flag register (IICF0)
STCF: Bit 7 of IIC flag register (IICF0)

16.4 Operation of DMA Controller

16.4.1 Operation procedure

<1> The DMA controller is enabled to operate when DENn = 1. Before writing the other registers, be sure to set DENn to 1. Use 80H to write with an 8-bit manipulation instruction.

<2> Set an SFR address, a RAM address, the number of times of transfer, and a transfer mode of DMA transfer to the DSAn, DRAn, CBCn, and DMCn registers.

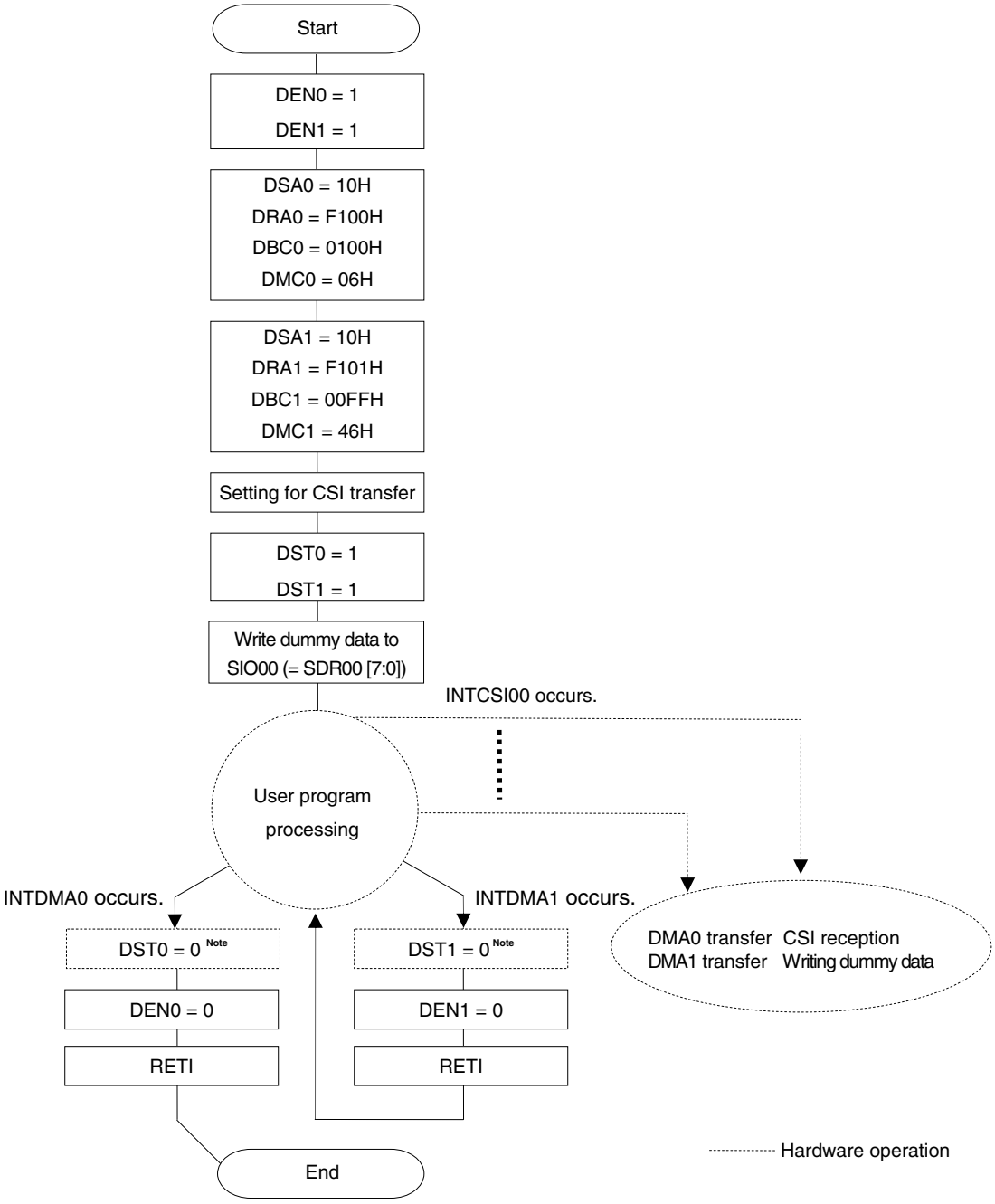
<3> The DMA controller waits for a DMA trigger when DSTn = 1. Use 81H to write with an 8-bit manipulation instruction.

<4> When a software trigger (STGn) or a start source trigger specified by IFCn3 to IFCn0 is input, a DMA transfer is started.

<5> Transfer is completed when the number of times of transfer set by the DBCn register reaches 0, and transfer is automatically terminated by occurrence of an interrupt (INTDMAn).

<6> Stop the operation of the DMA controller by clearing DENn to 0 when the DMA controller is not used.

Figure 16-8. Setting Example of CSI Master Reception



Note The DSTn flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DENn flag is enabled only when DSTn = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMAn (INTDMAn), set DSTn to 0 and then DENn to 0 (for details, refer to **16.5.7 Forcible termination by software**).

Because no CSI interrupt is generated when reception starts during CSI master reception, dummy data is written using software in this example.

The received data is automatically transferred from the first byte. (In successive reception mode, the data that is to be received when the first buffer empty interrupt occurs is invalid because the valid data has not been received.)

A DMA interrupt (INTDMA1) occurs when the last dummy data has been writing to the data register. A DMA interrupt (INTDMA0) occurs when the last received data has been read from the data register. To restart the DMA transfer, the CSI transfer must be completed.

16.5.7 Forced termination by software

After DSTn is set to 0 by software, it takes up to 2 clocks until a DMA transfer is actually stopped and DSTn is set to 0. To forcibly terminate a DMA transfer by software without waiting for occurrence of the interrupt (INTDMAn) of DMAn, therefore, perform either of the following processes.

<When using one DMA channel>

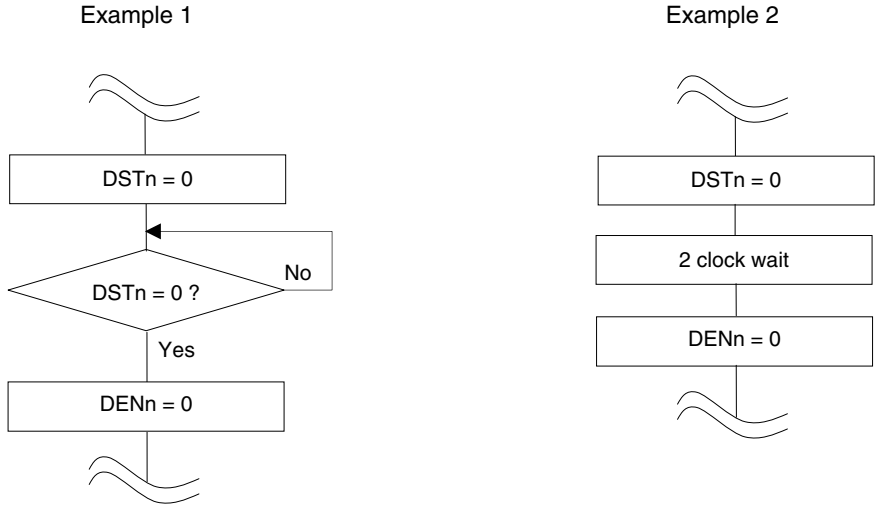
- Set DSTn to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software, confirm by polling that DSTn has actually been cleared to 0, and then set DENn to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction).

- Set DSTn to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software and then set DENn to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction) two or more clocks after.

<R> <When using both DMA channels>

- To forcibly terminate DMA transfer by software when using both DMA channels (by setting DSTn to 0), clear the DSTn bit to 0 after the DMA transfer is held pending by setting the DWAIT0 and DWAIT1 bits of both channels to 1. Next, clear the DWAIT0 and DWAIT1 bits of both channels to 0 to cancel the pending status, and then clear the DENn bit to 0.

Figure 16-13. Forced Termination of DMA Transfer (1/2)



Remarks 1. n: DMA channel number (n = 0, 1)

2. 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

Table 20-2. Hardware Statuses After Reset Acknowledgment (3/3)

Hardware		Status After Reset Acknowledgment[Note 1]
Serial interface IIC0	Shift register 0 (IIC0)	00H
	Control register 0 (IICC0)	00H
	Slave address register 0 (SVA0)	00H
	Clock select register 0 (IICCL0)	00H
	Function expansion register 0 (IICX0)	00H
	Status register 0 (IICS0)	00H
	Flag register 0 (IICF0)	00H
Multiplier	Multiplication input data register A (MULA)	0000H
	Multiplication input data register B (MULB)	0000H
	Higher multiplication result storage register (MULOH)	0000H
	Lower multiplication result storage register (MULOL)	0000H
Key interrupt	Key return mode register (KRM)	00H
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 3]
	Low-voltage detection level select register (LVIS)	0EH[Note 2]
Regulator	Regulator mode control register (RMC)	00H
DMA controller	SFR address registers 0, 1 (DSA0, DSA1)	00H
	RAM address registers 0L, 0H, 1L, 1H (DRA0L, DRA0H, DRA1L, DRA1H)	00H
	Byte count registers 0L, 0H, 1L, 1H (DBC0L, DBC0H, DBC1L, DBC1H)	00H
	Mode control registers 0, 1 (DMC0, DMC1)	00H
	Operation control registers 0, 1 (DRC0, DRC1)	00H
Interrupt	Request flag registers 0L, 0H, 1L, 1H, 2L, 2H (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)	00H
	Mask flag registers 0L, 0H, 1L, 1H, 2L, 2H (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)	FFH
	Priority specification flag registers 00L, 00H, 01L, 01H, 02L, 02H, 10L, 10H, 11L, 11H, 12L, 12H (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR02L, PR02H, PR12L, PR12H)	FFH
	External interrupt rising edge enable registers 0, 1 (EGP0, EGP1)	00H
	External interrupt falling edge enable registers 0, 1 (EGN0, EGN1)	00H
BCD correction circuit	BCD correction result register (BCDADJ)	Undefined

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by LVI
RESF	TRAP bit	Cleared (0)	Cleared (0)	Set (1)	Held	Held
	WDRF bit			Held	Set (1)	Held
	LVIRF bit			Held	Held	Set (1)
LVIS		Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Held

3. This value varies depending on the reset source and the option byte.

(5) XT1 oscillation: Crystal resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (kHz)	Load Capacitance CL (pF)	Recommended Circuit Constants			Oscillation Voltage Range	
					C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Seiko Instruments Inc.	SP-T2A	SMD	32.768	6.0	5	5	0	1.8	5.5
				12.5	18	18	0		
	SSP-T7	Small SMD		7.0	7	7	0		
				12.5	18	18	0		
	VT-200	Lead		6.0	5	5	0		
				12.5	18	18	0		
CITIZEN FINETECH MIYOTA CO., LTD.	CM200S	SMD	32.768	9.0	12	15	0	1.8	5.5
					12	15	100		
	CM315	SMD		9.0	15	15	0		
					15	15	100		
	CM519	SMD		9.0	15	12	0		
					15	12	100		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KG3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(6) XT1 oscillation: Crystal resonator (T_A = –20 to +70°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (kHz)	Load Capacitance CL (pF)	Recommended Circuit Constants			Oscillation Voltage Range	
					C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
CITIZEN FINETECH MIYOTA CO., LTD.	CFS-206	Lead	32.768	12.5	22	18	0	1.8	5.5
					22	18	100		
				9.0	12	15	0		
					12	15	100		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KG3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(2) External bus interface (3/3)

(b) Read/write cycle (CLKOUT asynchronous)

- **Conventional-specification products (μPD78F116x)**

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle	t_{CYK2}	<18>	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
$\overline{RD}$ low-level width	t_{WRDL2}	<19>	2.7 V ≤ V_{DD} ≤ 5.5 V	$1.8t_{CYK2}$ – 40		$2.2t_{CYK2}$	ns
$\overline{WR0}$, $\overline{WR1}$ low-level width	t_{WWRL2}	<20>	2.7 V ≤ V_{DD} ≤ 5.5 V	$0.8t_{CYK2}$ – 40		$1.2t_{CYK2}$	ns
Data input setup time to $\overline{RD}$↑	t_{SRDDI2}	<21>	2.7 V ≤ V_{DD} ≤ 5.5 V	90			ns
Data input hold time from $\overline{RD}$↑	t_{HRDDI2}	<22>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
Data output setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWROD2}	<23>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns
Data output hold time from $\overline{WR0}$, $\overline{WR1}$↑	t_{HKOD2}	<24>	2.7 V ≤ V_{DD} ≤ 5.5 V	2			ns
Delay time from $\overline{RD}$↓ to address	t_{DRDA2}	<25>	2.7 V ≤ V_{DD} ≤ 5.5 V			5	ns
Address setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWRA2}	<26>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns

- **Expanded-specification products (μPD78F116xA)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle	t_{CYK2}	<18>	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
			1.8 V ≤ V_{DD} < 2.7 V	200			ns
$\overline{RD}$ low-level width	t_{WRDL2}	<19>	2.7 V ≤ V_{DD} ≤ 5.5 V	$1.8t_{CYK2}$ – 40		$2.2t_{CYK2}$	ns
			1.8 V ≤ V_{DD} < 2.7 V	$1.8t_{CYK2}$ – 60		$2.2t_{CYK2}$	ns
$\overline{WR0}$, $\overline{WR1}$ low-level width	t_{WWRL2}	<20>	2.7 V ≤ V_{DD} ≤ 5.5 V	$0.8t_{CYK2}$ – 40		$1.2t_{CYK2}$	ns
			1.8 V ≤ V_{DD} < 2.7 V	$0.8t_{CYK2}$ – 60		$1.2t_{CYK2}$	ns
Data input setup time to $\overline{RD}$↑	t_{SRDDI2}	<21>	2.7 V ≤ V_{DD} ≤ 5.5 V	90			ns
			1.8 V ≤ V_{DD} < 2.7 V	170			ns
Data input hold time from $\overline{RD}$↑	t_{HRDDI2}	<22>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
			1.8 V ≤ V_{DD} < 2.7 V	0			ns
Data output setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWROD2}	<23>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns
			1.8 V ≤ V_{DD} < 2.7 V	t_{CYK2} – 15			ns
Data output hold time from $\overline{WR0}$, $\overline{WR1}$↑	t_{HKOD2}	<24>	2.7 V ≤ V_{DD} ≤ 5.5 V	2			ns
			1.8 V ≤ V_{DD} < 2.7 V	2			ns
Delay time from $\overline{RD}$↓ to address	t_{DRDA2}	<25>	2.7 V ≤ V_{DD} ≤ 5.5 V			5	ns
			1.8 V ≤ V_{DD} < 2.7 V			15	ns
Address setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWRA2}	<26>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns
			1.8 V ≤ V_{DD} < 2.7 V	t_{CYK2} – 15			ns

Cautions 1. CLKOUT output is not used during CLKOUT asynchronous operation, but a CPU wait occurs according to the setting of bits 4 and 5 (EW0, EW1) of the memory expansion mode control register (MEM). When f_{CLK} is sufficiently high, insert a wait by setting the EW0 and EW1 bits.

2. Do not use the $\overline{WAIT}$ pin during CLKOUT asynchronous operation.
Use the separate bus mode during CLKOUT asynchronous operation.

Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency

2. C_L: The pin load capacitance is 15 pF.

3. Test points: V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

(3) Serial interface: Serial array unit (15/18)

Caution Select the TTL input buffer for SIp and $\overline{SCKp}$ and the N-ch open-drain output (V_{DD} tolerance) mode for SOp by using the PIMg and POMg registers.

Remarks 1. p: CSI number (p = 01, 10, 20), g: PIM and POM number (g = 0, 4, 14)

2. R_b[Ω]: Communication line (SOp) pull-up resistance,
C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of the SMRmn register. m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 2))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$: $V_{IH} = 2.2\ V$, $V_{IL} = 0.8\ V$

$2.7\ V \le V_{DD} \le 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

5. CSI00 cannot communicate at different potential. Use CSI01, CSI10, and CSI20 for communication at different potential.

A/D Converter Characteristics

(T_A = –40 to +85°C, 2.3 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 2.3 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				10	bit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.5	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.7	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF0} ≤ 5.5 V	6.1		66.6	μs
		2.7 V ≤ AV_{REF0} < 4.0 V	12.2		66.6	μs
		2.3 V ≤ AV_{REF0} < 2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	EZS	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.5	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.5	%FSR
Full-scale error[Notes 1, 2]	EFS	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.5	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.5	%FSR
Integral linearity error[Note 1]	ILE	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF0} < 4.0 V			±3.5	LSB
		2.3 V ≤ AV_{REF0} < 2.7 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF0} < 4.0 V			±1.5	LSB
		2.3 V ≤ AV_{REF0} < 2.7 V			±1.5	LSB
Analog input voltage	V_{AIN}	2.3 V ≤ AV_{REF0} ≤ 5.5 V	AV_{SS}		AV_{REF0}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 11	Soft	A/D converter	A/D conversion result register (ADCR, ADCRH) read operation	When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.	p.378 ☐
			A/D conversion result register (ADCR, ADCRH) read operation	When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.	p.378 ☐
			Starting the A/D converter	Start the A/D converter after the AV_{REF0} and AV_{REF1} voltages (the reference voltages for the D/A converter) stabilize.	p.379 ☐
Chapter 12	Soft	D/A converter	PER0: Peripheral enable register 0	When setting the D/A converter, be sure to set DACEN to 1 first. If DACEN = 0, writing to a control register of the D/A converter is ignored, and, even if the register is read, only the default value is read (except for port mode register 11 (PM11) and port register 11 (P11)).	p.382 ☐
				Be sure to clear bit 1 of the PER0 register to 0.	p.382 ☐
			Operation in normal mode	Make the interval for writing DACSn of the same channel by one clock longer than f_{CLK}. If writing is successively performed, only the value written last will be converted.	p.385 ☐
			Operation in real-time output mode	Make the interval for generating a start trigger to the same channel by one clock longer than f_{CLK}. If a start trigger is successively generated for every f_{CLK}, D/A conversion will be performed only at the first trigger.	p.386 ☐
				Note the following points in the procedure (i to iii) for outputting an arbitrary value in <3>. • Do not generate the start trigger of the real-time output mode before enabling D/A conversion operation in <3> after the value is set to the DACSn register in ii. • An arbitrary value cannot be output in <3> if the DACEN bit of the PER0 register is cleared once after the value is set to the DACSn register in ii.	p.386 ☐
			I/O function of digital ports alternately used as ANO0, ANO1	The digital port I/O function, which is the alternate function of the ANO0 and ANO1 pins, does not operate during D/A conversion. During D/A conversion, 0 is read from the P11 register in input mode.	p.387 ☐
			P11, PM11 registers	Do not read/write the P11 register and do not change the setting of the PM11 register during D/A conversion (otherwise the conversion accuracy may decrease).	p.387 ☐
			ANO0, ANO1 pins	It is recommended that both the ANO0 and ANO1 pins be used as analog output pins or digital I/O pins, that is, use these two channels for the same application (if these pins are used for the different applications, the conversion accuracy may decrease).	p.387 ☐
			DACSn register	In the real-time output mode, set the DACSn register value before the timer trigger is generated. In addition, do not change the set value of the DACSn register while the trigger signal is output.	p.387 ☐
			Changing operation mode	Before changing the operation mode, be sure to clear the DACEn bit of the DAM register to 0 (D/A conversion stop).	p.387 ☐
	Hard		Port alternately used as ANO0 or ANO1 pin	When using the port that functions alternately as the ANO0 or ANO1 pin, use it as the port input with few level changes.	p.387 ☐
			Applying power to and disconnecting power from AV_{REF1} and AV_{REF0}	Stop the conversion performed by the D/A converter when supplying AV_{REF1} or AV_{REF0} (the reference voltages for the A/D converter) starts or stops.	p.387 ☐

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Edition	Description	Chapter
8th edition	Modification of **Figure 13-36 Timing Chart of Master Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	CHAPTER 13 SERIAL ARRAY UNIT
	Change of **Figure 13-40 Procedure for Stopping Master Transmission/Reception**	
	Change of **Figure 13-41 Procedure for Resuming Master Transmission/Reception**	
	Modification of **Figure 13-42 Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-44 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-45 Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**	
	Change of transfer rate in **13.5.4 Slave transmission**	
	Change of **Figure 13-48 Procedure for Stopping Slave Transmission**	
	Change of **Figure 13-49 Procedure for Resuming Slave Transmission**	
	Change of **Figure 13-50 Timing Chart of Slave Transmission (in Single-Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of **Figure 13-52 Timing Chart of Slave Transmission (in Continuous Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of **Figure 13-53 Flowchart of Slave Transmission (in Continuous Transmission Mode)**	
	Change of transfer rate in **13.5.5 Slave reception**	
	Change of **Figure 13-57 Procedure for Resuming Slave Reception**	
	Modification of **Figure 13-58 Timing Chart of Slave Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of transfer rate in **13.5.6 Slave transmission/reception**	
	Change of **Figure 13-62 Procedure for Stopping Slave Transmission/Reception**	
	Change of **Figure 13-63 Procedure for Resuming Slave Transmission/Reception**	
	Modification of **Figure 13-64 Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-66 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-67 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**	
	Change of **Note 2** in **Table 13-2 Selection of Operation Clock**	
	Addition of **Caution** to **13.6 Operation of UART (UART0, UART1, UART2, UART3) Communication**	
	Change of **Figure 13-70 Procedure for Stopping UART Transmission**	
	Change of **Figure 13-72 Timing Chart of UART Transmission (in Single-Transmission Mode)**	
	Change of **Figure 13-74 Timing Chart of UART Transmission (in Continuous Transmission Mode)**	
	Change of **13.6.2 UART reception**	
	Change of **(b) Serial output enable register m (SOEm)** in **Figure 13-76 Example of Contents of Registers for UART Reception of UART (UART0, UART1, UART2, UART3)**	
	Modification of **Figure 13-80 Timing Chart of UART Reception**	
	Modification of transfer data length in **13.6.3 LIN transmission**	
	Change of **Note 2** in **Figure 13-82 Transmission Operation of LIN**	