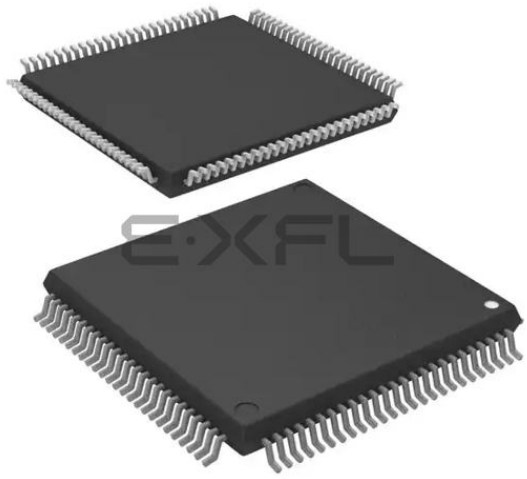
Renesas Electronics America Inc - UPD78F1163AGF-GAS-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1163agf-gas-ax

RENESAS

User's Manual

78K0R/KG3

16-bit Single-Chip Microcontrollers

μPD78F1162, 78F1162A, 78F1162A(A)
μPD78F1163, 78F1163A, 78F1163A(A)
μPD78F1164, 78F1164A, 78F1164A(A)
μPD78F1165, 78F1165A, 78F1165A(A)
μPD78F1166, 78F1166A, 78F1166A(A)
μPD78F1167, 78F1167A, 78F1167A(A)
μPD78F1168, 78F1168A, 78F1168A(A)

Document No. U17894EJ9V0UD00 (9th edition)
Date Published July 2009 NS

(c) TOOL1

This is a clock output pin for a debugger.

When the on-chip debug function is used, P41/TOOL1 pin can be used as follows by the mode setting on the debugger.

1-line mode: can be used as a port (P41).

2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).

(d) TI04, TI05

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 04 and 05.

(e) TO04, TO05

These are the timer output pins from 16-bit timers 04 and 05.

(f) $\overline{\text{SCK01}}$

This is a serial clock I/O pin of serial interface CSI01.

(g) SI01

This is a serial data input pin of serial interface CSI01.

(h) SO01

This is a serial data output pin of serial interface CSI01.

Caution The function of the P40/TOOL0 pin varies as described in (a) to (c) below.
In the case of (b) or (c), make the specified connection.

(a) In normal operation mode and when on-chip debugging is disabled (OCDENSET = 0) by an option byte (000C3H)
=> Use this pin as a port pin (P40).

(b) In normal operation mode and when on-chip debugging is enabled (OCDENSET = 1) by an option byte (000C3H)
=> Connect this pin to EV_{DD0} or EV_{DD1} via an external resistor, and always input a high level to the pin before reset release.

(c) When on-chip debug function is used, or in write mode of flash memory programmer
=> Use this pin as TOOL0.
Directly connect this pin to the on-chip debug emulator or a flash memory programmer, or pull it up by connecting it to EV_{DD0} or EV_{DD1} via an external resistor.

2.2.6 P50 to P57 (port 5)

P50 to P57 function as an 8-bit I/O port. These pins also function as external expansion I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P50 to P57 function as an 8-bit I/O port. P50 to P57 can be set to input or output port in 1-bit units using port mode register 5 (PM5). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 5 (PU5).

3.3.4 Register direct addressing

[Function]

Register direct addressing stores in the program counter (PC) the contents of a general-purpose register pair (AX/BC/DE/HL) and CS register of the current register bank specified with the instruction word as 20-bit data, and specifies the program address. Register direct addressing can be applied only to the CALL AX, BC, DE, HL, and BR AX instructions.

Figure 3-26. Outline of Register Direct Addressing

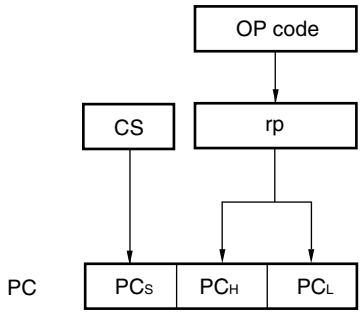


Figure 7-6. Format of Timer Mode Register 0n (TMR0n) (3/3)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR0n	CKS 0n	0	0	CCS 0n	MAST ER0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0

MD 0n3	MD 0n2	MD 0n1	MD 0n0	Operation mode of channel n	Count operation of TCR	Independent operation
0	0	0	1/0	Interval timer mode	Counting down	Possible
0	1	0	1/0	Capture mode	Counting up	Possible
0	1	1	0	Event counter mode	Counting down	Possible
1	0	0	1/0	One-count mode	Counting down	Impossible
1	1	0	0	Capture & one-count mode	Counting up	Possible
Other than above				Setting prohibited		
The operation of MD0n0 bits varies depending on each operation mode (see table below).						

Operation mode (Value set by the MD0n3 to MD0n1 bits (see table above))	MD 0n0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation[Note]. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Note If the start trigger (TS0n = 1) is issued during operation, the counter is cleared, an interrupt is generated, and recounting is started.

Remark n = 0 to 7

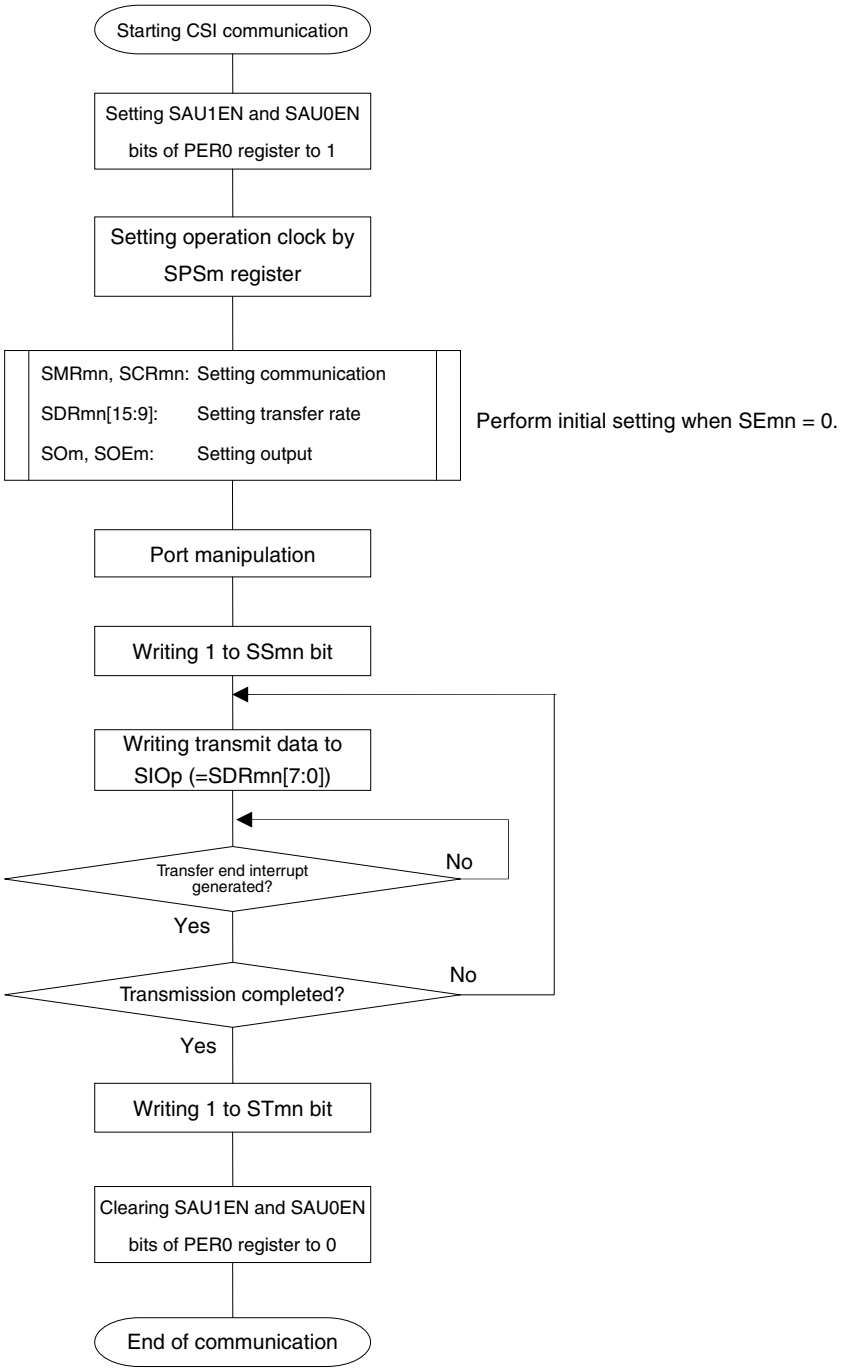
Figure 7-69. Operation Procedure When Multiple PWM Output Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit of the PER0 register to 1. ⟶	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPS0 register. Determines clock frequencies of CK00 and CK01.	
Channel default setting	Sets the TMR0n, TMR0p, and TMR0q registers of each channel to be used (determines operation mode of channels). An interval (period) value is set to the TDR0n register of the master channel, and a duty factor is set to the TDR0p and TDR0q registers of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOM0p and TOM0q bits of the TOM0 register are set to 1 (combination operation mode). Clears the TOL0p and TOL0q bits to 0. Sets the TO0p and TO0q bits and determines default level of the TO0p and TO0q outputs. ⟶	The TO0p and TO0q pins go into Hi-Z output state. The TO0p and TO0q default setting levels are output when the port mode register is in output mode and the port register is 0.
	Sets TOE0p or TOE0q to 1 and enables operation of TO0p or TO0q. ⟶	TO0p or TO0q does not change because channel stops operating.
	Clears the port register and port mode register to 0. ⟶	The TO0p and TO0q pins output the TO0p and TO0q set levels.

Remarks 1. n = 0, 2, 4

2. p = n + 1; q = n + 2

Figure 13-29. Flowchart of Master Transmission (in Single-Transmission Mode)



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

13.5.3 Master transmission/reception

Master transmission/reception is an operation in which the 78K0R/KG3 outputs a transfer clock and transmits/receives data to/from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	$\overline{\text{SCK00}}$, SI00, SO00	$\overline{\text{SCK01}}$, SI01, SO01	$\overline{\text{SCK10}}$, SI10, SO10	$\overline{\text{SCK20}}$, SI20, SO20
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.			
Error detection flag	Overrun error detection flag (OVFmn) only			
Transfer data length	7 or 8 bits			
Transfer rate	Max. $f_{CLK}/4$ [Hz], Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [Hz]Note f_{CLK}: System clock frequency			
Data phase	Selectable by DAPmn bit • DAPmn = 0: Data I/O starts at the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.			
Clock phase	Selectable by CKPmn bit • CKPmn = 0: Forward • CKPmn = 1: Reverse			
Data direction	MSB or LSB first			

Note Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)** and **CHAPTER 30 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

Table 13-6. Relationship Between Register Settings and Pins (Channel 1 of Unit 0: CSI01, UART0 Reception)

SE 01 Note 1	MD 012	MD 011	SOE 01	SO01	CKO 01	TXE 01	RXE 01	PM 43	P43	PM44	P44	PM 45	P45	PM 11 Note 2	P11 Note 2	Operation Mode	Pin Function			
																	$\overline{\text{SCK01}}$/ P43	SI01/P44	SO01/ P45	SI00/EX25/ RxD0/ P11 Note 2
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	P43	P44	P45	SI00/EX25/ P11
	0	1																		
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Slave CSI01 reception	$\overline{\text{SCK01}}$ (input)	SI01	P45	SI00/EX25/ P11
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Slave CSI01 transmission	$\overline{\text{SCK01}}$ (input)	P44	SO01	SI00/EX25/ P11
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	× Note 3	× Note 3	Slave CSI01 transmission /reception	$\overline{\text{SCK01}}$ (input)	SI01	SO01	SI00/EX25/ P11
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Master CSI01 reception	$\overline{\text{SCK01}}$ (output)	SI01	P45	SI00/EX25/ P11
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Master CSI01 transmission	$\overline{\text{SCK01}}$ (output)	P44	SO01	SI00/EX25/ P11
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	× Note 3	× Note 3	Master CSI01 transmission /reception	$\overline{\text{SCK01}}$ (output)	SI01	SO01	SI00/EX25/ P11
	0	1	0	1	1	0	1	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	1	×	UART0 reception Notes 5, 6	P43	P44	P45	RxD0

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. When channel 1 of unit 0 is set to UART0 reception, this pin becomes an RxD0 function pin. In this case, set channel 0 of unit 0 to operation stop mode or UART0 transmission (refer to **Table 13-5**).
When channel 0 of unit 0 is set to CSI00, this pin cannot be used as an RxD0 function pin. In this case, set channel 1 of unit 0 to operation stop mode or CSI01.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **13.3 (12) Serial output register m (SOm)**.

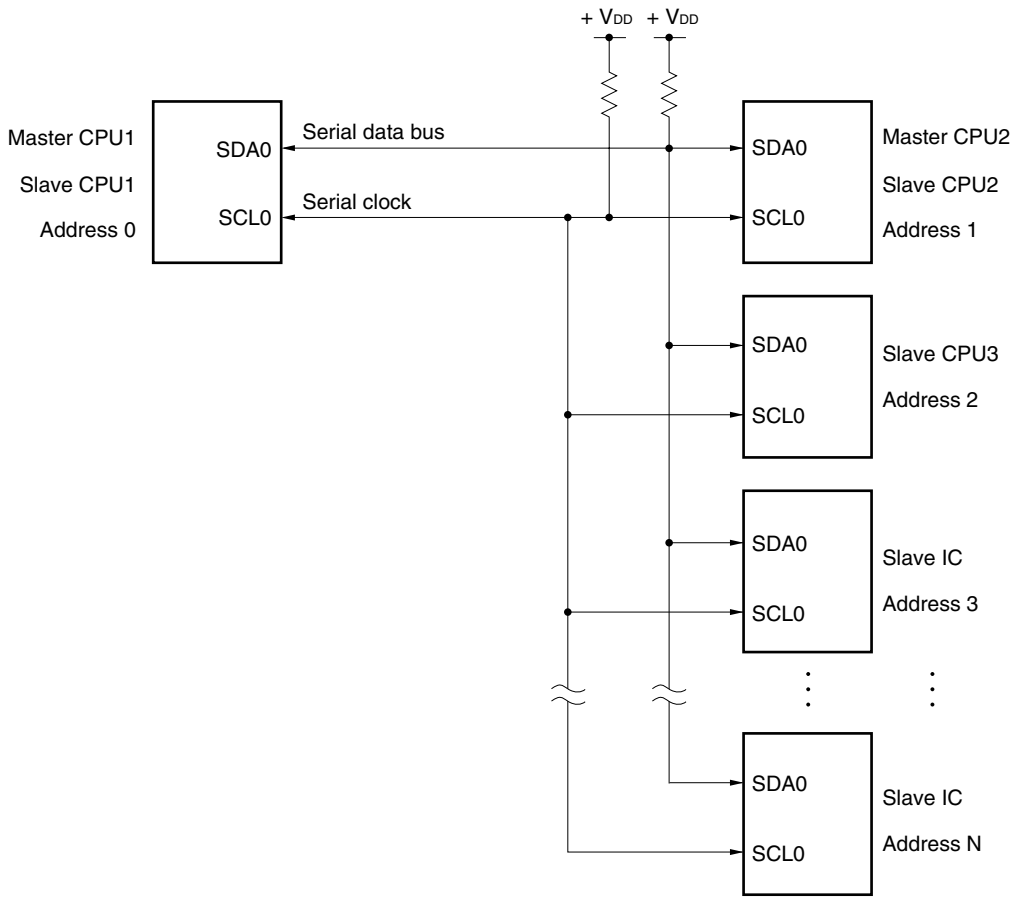
5. When using UART0 transmission and reception in a pair, set channel 0 of unit 0 to UART0 transmission (refer to **Table 13-5**).

6. The SMR00 register of channel 0 of unit 0 must also be set during UART0 reception. For details, refer to **13.6.2 (1) Register setting**.

Remark X: Don't care

Figure 14-2 shows a serial bus configuration example.

Figure 14-2. Serial Bus Configuration Example Using I^2C Bus



(7) Port mode register 6 (PM6)

This register sets the input/output of port 6 in 1-bit units.

When using the P60/SCL0 pin as clock I/O and the P61/SDA0 pin as serial data I/O, clear PM60 and PM61, and the output latches of P60 and P61 to 0.

Set IICE0 (bit 7 of IIC control register 0 (IICC0)) to 1 before setting the output mode because the P60/SCL0 and P61/SDA0 pins output a low level (fixed) when IICE0 is 0.

PM6 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 14-11. Format of Port Mode Register 6 (PM6)

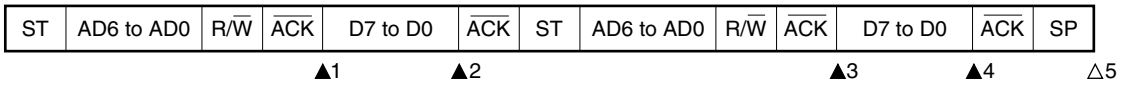
Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60

PM6n	P6n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

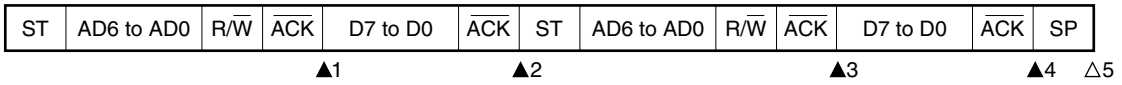
(i) When WTIM0 = 0 (after restart, matches with SVA0)



▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×000B
▲3: IICS0 = 0001×110B
▲4: IICS0 = 0001×000B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches with SVA0)



▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001××00B
▲3: IICS0 = 0001×110B
▲4: IICS0 = 0001××00B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

14.6 Timing Charts

When using the I^2C bus mode, the master device outputs an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the TRC0 bit (bit 3 of IIC status register 0 (IICS0)), which specifies the data transfer direction, and then starts serial communication with the slave device.

Figures 14-28 and 14-29 show timing charts of the data communication.

The shift operation of IIC shift register 0 (IIC0) is synchronized with the falling edge of the serial clock (SCL0). The transmit data is transferred to the SO0 latch and is output (MSB first) via the SDA0 pin.

Data input via the SDA0 pin is captured into IIC0 at the rising edge of SCL0.

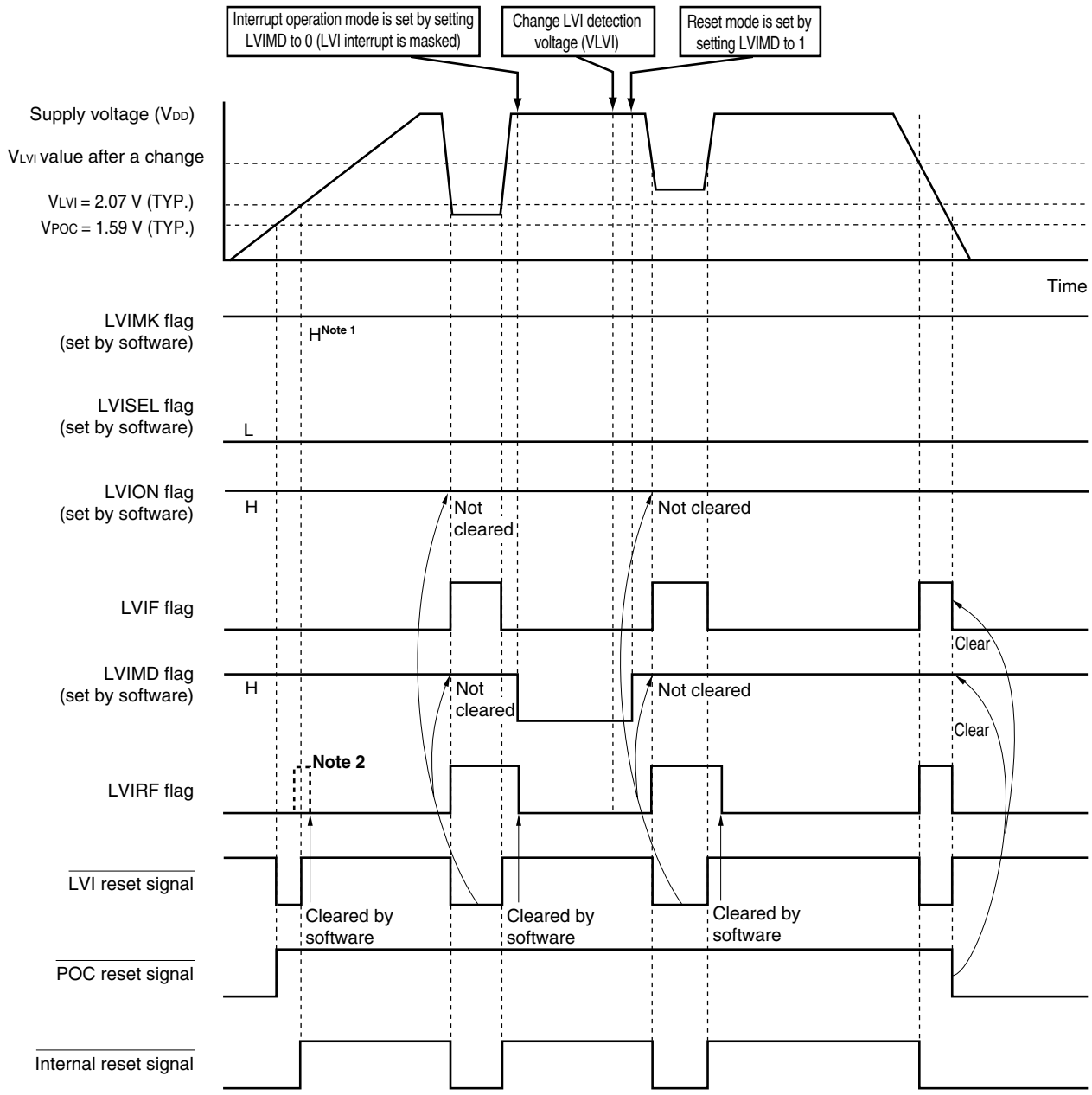
Table 20-2. Hardware Statuses After Reset Acknowledgment (1/3)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers (P0 to P8, P11 to P15) (output latches)		00H
Port mode registers	PM0 to PM8, PM11, PM12, PM14, PM15	FFH
	PM13	FEH
Port input mode registers 0, 4, 14 (PIM0, PIM4, PIM14)		00H
Port output mode registers 0, 4, 14 (POM0, POM4, POM14)		00H
Pull-up resistor option registers (PU0, PU1, PU3 to PU8, PU12 to PU14)		00H
Memory extension mode control register (MEM)		00H
Clock operation mode control register (CMC)		00H
Clock operation status control register (CSC)		C0H
Processor mode control register (PMC)		00H
System clock control register (CKC)		09H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		07H
Noise filter enable registers 0, 1 (NFEN0, NFEN1)		00H
Peripheral enable registers 0, 1 (PER0, PER1)		00H
Internal high-speed oscillator trimming register (HIOTRM)		10H
Operation speed mode control register (OSMC)		00H
Timer array unit (TAU)	Timer data registers 00, 01, 02, 03, 04, 05, 06, 07 (TDR00, TDR01, TDR02, TDR03, TDR04, TDR05, TDR06, TDR07)	0000H
	Timer mode registers 00, 01, 02, 03, 04, 05, 06, 07 (TMR00, TMR01, TMR02, TMR03, TMR04, TMR05, TMR06, TMR07)	0000H
	Timer status registers 00, 01, 02, 03, 04, 05, 06, 07 (TSR00, TSR01, TSR02, TSR03, TSR04, TSR05, TSR06, TSR07)	0000H
	Timer input select register 0 (TIS0)	00H
	Timer counter registers 00, 01, 02, 03, 04, 05, 06, 07 (TCR00, TCR01, TCR02, TCR03, TCR04, TCR05, TCR06, TCR07)	FFFFH
	Timer channel enable status register 0 (TE0)	0000H
	Timer channel start register 0 (TS0)	0000H
	Timer channel stop register 0 (TT0)	0000H
	Timer clock select register 0 (TPS0)	0000H
	Timer output register 0 (TO0)	0000H
	Timer output enable register 0 (TOE0)	0000H
	Timer output level register 0 (TOL0)	0000H
	Timer output mode register 0 (TOM0)	0000H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

Figure 22-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 0)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. LVIRF is bit 0 of the reset control flag register (RESF).

When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, the LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of RESF, see **CHAPTER 20 RESET FUNCTION**.

24.4 Setting of Option Byte

The user option byte and on-chip debug option byte can be set using the RA78K0R or PM+ linker option, in addition to describing to the source. When doing so, the contents set by using the linker option take precedence, even if descriptions exist in the source, as mentioned below.

See the **RA78K0R Assembler Package User's Manual** for how to set the linker option.

A software description example of the option byte setting is shown below.

```
OPT   CSEG       OPT_BYTE
      DB         10H     ; Does not use interval interrupt of watchdog timer,
                         ; Enables watchdog timer operation,
                         ; Window open period of watchdog timer is 25%,
                         ; Overflow time of watchdog timer is 2^10/fIL,
                         ; Stops watchdog timer operation during HALT/STOP mode
      DB         0FFH    ; Stops LVI default start function
      DB         0FFH    ; Reserved area
      DB         85H     ; Enables on-chip debug operation, does not erase flash memory
                         ; data when security ID authorization fails
```

When the boot swap function is used during self programming, 000C0H to 000C3H is switched to 010C0H to 010C3H. Describe to 010C0H to 010C3H, therefore, the same values as 000C0H to 000C3H as follows.

```
OPT2  CSEG   AT   010C0H
      DB         10H     ; Does not use interval interrupt of watchdog timer,
                         ; Enables watchdog timer operation,
                         ; Window open period of watchdog timer is 25%,
                         ; Overflow time of watchdog timer is 2^10/fIL,
                         ; Stops watchdog timer operation during HALT/STOP mode
      DB         0FFH    ; Stops LVI default start function
      DB         0FFH    ; Reserved area
      DB         85H     ; Enables on-chip debug operation, does not erase flash memory
                         ; data when security ID authorization fails
```

Caution To specify the option byte by using assembly language, use OPT_BYTE as the relocation attribute name of the CSEG pseudo instruction. To specify the option byte to 010C0H to 010C3H in order to use the boot swap function, use the relocation attribute AT to specify an absolute address.

(3) X1 oscillation: Ceramic resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd.	CSTCE12M0G55-R0	SMD	12.0	Internal (33)	Internal (33)	1.8	5.5
	CSTCE16M0V53-R0	SMD	16.0	Internal (15)	Internal (15)	1.8	
	CSTLS16M0X51-B0	Lead		Internal (5)	Internal (5)	1.8	
	CSTCE20M0V53-R0	SMD	20.0	Internal (15)	Internal (15)	1.9	
	CSTCG20M0V53-R0	Small SMD		Internal (15)	Internal (15)	2.0	
	CSTLS20M0X51-B0	Lead		Internal (5)	Internal (5)	1.9	
TOKO, Inc.	DCRHYC(P)12.00A	Lead	12.0	Internal (22)	Internal (22)	1.8	5.5
	DCRHZ(P)16.00A-15	Lead	16.0	Internal (15)	Internal (15)		
	DCRHZ(P)20.00A-15	Lead	20.0	Internal (15)	Internal (15)	2.0	
	DECRHZ20.00	SMD		Internal (10)	Internal (10)	1.8	

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KG3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(2) External bus interface (3/3)

(b) Read/write cycle (CLKOUT asynchronous)

- **Conventional-specification products (μPD78F116x)**

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle	t_{CYK2}	<18>	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
$\overline{RD}$ low-level width	t_{WRDL2}	<19>	2.7 V ≤ V_{DD} ≤ 5.5 V	$1.8t_{CYK2}$ – 40		$2.2t_{CYK2}$	ns
$\overline{WR0}$, $\overline{WR1}$ low-level width	t_{WWRL2}	<20>	2.7 V ≤ V_{DD} ≤ 5.5 V	$0.8t_{CYK2}$ – 40		$1.2t_{CYK2}$	ns
Data input setup time to $\overline{RD}$↑	t_{SRDDI2}	<21>	2.7 V ≤ V_{DD} ≤ 5.5 V	90			ns
Data input hold time from $\overline{RD}$↑	t_{HRDDI2}	<22>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
Data output setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWROD2}	<23>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns
Data output hold time from $\overline{WR0}$, $\overline{WR1}$↑	t_{HKOD2}	<24>	2.7 V ≤ V_{DD} ≤ 5.5 V	2			ns
Delay time from $\overline{RD}$↓ to address	t_{DRDA2}	<25>	2.7 V ≤ V_{DD} ≤ 5.5 V			5	ns
Address setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWRA2}	<26>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns

- **Expanded-specification products (μPD78F116xA)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle	t_{CYK2}	<18>	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
			1.8 V ≤ V_{DD} < 2.7 V	200			ns
$\overline{RD}$ low-level width	t_{WRDL2}	<19>	2.7 V ≤ V_{DD} ≤ 5.5 V	$1.8t_{CYK2}$ – 40		$2.2t_{CYK2}$	ns
			1.8 V ≤ V_{DD} < 2.7 V	$1.8t_{CYK2}$ – 60		$2.2t_{CYK2}$	ns
$\overline{WR0}$, $\overline{WR1}$ low-level width	t_{WWRL2}	<20>	2.7 V ≤ V_{DD} ≤ 5.5 V	$0.8t_{CYK2}$ – 40		$1.2t_{CYK2}$	ns
			1.8 V ≤ V_{DD} < 2.7 V	$0.8t_{CYK2}$ – 60		$1.2t_{CYK2}$	ns
Data input setup time to $\overline{RD}$↑	t_{SRDDI2}	<21>	2.7 V ≤ V_{DD} ≤ 5.5 V	90			ns
			1.8 V ≤ V_{DD} < 2.7 V	170			ns
Data input hold time from $\overline{RD}$↑	t_{HRDDI2}	<22>	2.7 V ≤ V_{DD} ≤ 5.5 V	0			ns
			1.8 V ≤ V_{DD} < 2.7 V	0			ns
Data output setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWROD2}	<23>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns
			1.8 V ≤ V_{DD} < 2.7 V	t_{CYK2} – 15			ns
Data output hold time from $\overline{WR0}$, $\overline{WR1}$↑	t_{HKOD2}	<24>	2.7 V ≤ V_{DD} ≤ 5.5 V	2			ns
			1.8 V ≤ V_{DD} < 2.7 V	2			ns
Delay time from $\overline{RD}$↓ to address	t_{DRDA2}	<25>	2.7 V ≤ V_{DD} ≤ 5.5 V			5	ns
			1.8 V ≤ V_{DD} < 2.7 V			15	ns
Address setup time to $\overline{WR0}$, $\overline{WR1}$↓	t_{SWRA2}	<26>	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{CYK2} – 5			ns
			1.8 V ≤ V_{DD} < 2.7 V	t_{CYK2} – 15			ns

Cautions 1. CLKOUT output is not used during CLKOUT asynchronous operation, but a CPU wait occurs according to the setting of bits 4 and 5 (EW0, EW1) of the memory expansion mode control register (MEM). When f_{CLK} is sufficiently high, insert a wait by setting the EW0 and EW1 bits.

2. Do not use the $\overline{WAIT}$ pin during CLKOUT asynchronous operation.
Use the separate bus mode during CLKOUT asynchronous operation.

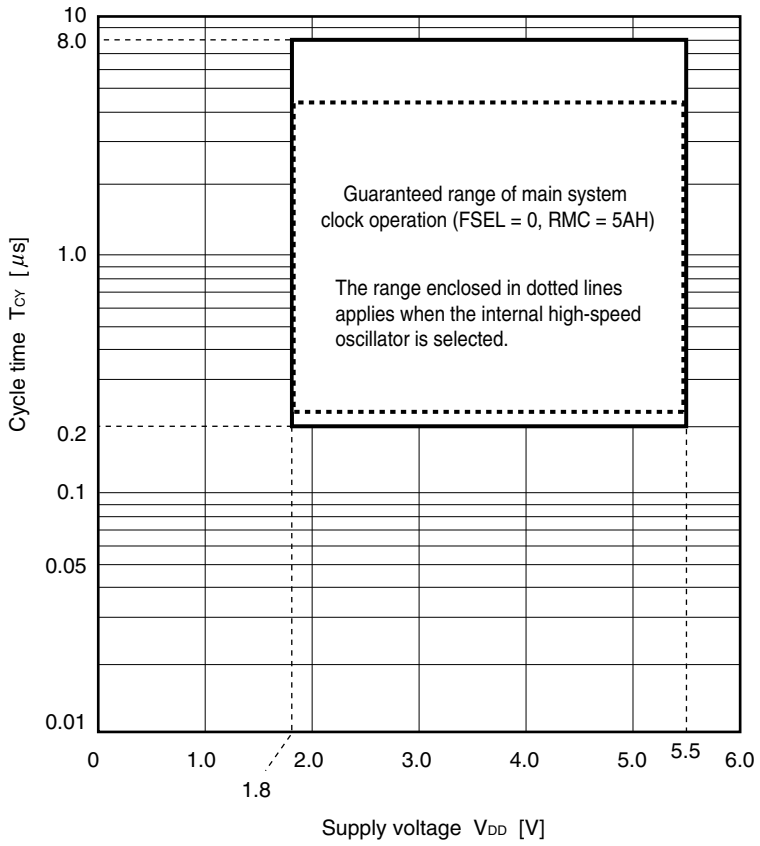
Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency

2. C_L: The pin load capacitance is 15 pF.

3. Test points: V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

(1) Basic operation (4/6)

Minimum instruction execution time during main system clock operation (FSEL = 0, RMC = 5AH)



Remarks 1. FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register

2. The entire voltage range is 5 MHz (MAX.) when RMC is set to 5AH.

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 30	Soft	Electrical specifications ((A) grade products)	During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock input)	Select the normal input buffer for SIj and the normal output mode for SOj and $\overline{\text{SCKj}}$ by using the PIMg and POMg registers.	p.864 ☐
			During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)	Select the normal input buffer for SIj and $\overline{\text{SCKj}}$ and the normal output mode for SOj by using the PIMg and POMg registers.	p.865 ☐
			During communication at same potential (simplified I^2C mode)	Select the normal input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDAr and the normal output mode for SCLr by using the PIMg and POMg registers.	p.868 ☐
			During communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)	Select the TTL input buffer for RxDq and the N-ch open-drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMg registers.	pp.869, 870, 872 ☐
			During communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output)	Select the TTL input buffer for SIp and the N-ch open-drain output (V_{DD} tolerance) mode for SOp and $\overline{\text{SCKp}}$ by using the PIMg and POMg registers.	pp.873, 874, 875 ☐
			During communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)	Select the TTL input buffer for SIp and $\overline{\text{SCKp}}$ and the N-ch open-drain output (V_{DD} tolerance) mode for SOp by using the PIMg and POMg registers.	pp.877, 878 ☐
			During communication at different potential (2.5 V, 3 V) (simplified I^2C mode)	Select the TTL input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDAr and the N-ch open-drain output (V_{DD} tolerance) mode for SCLr by using the PIMg and POMg registers.	pp.879, 880 ☐

(14/24)

Edition	Description	Chapter
5th edition	Change of transfer rate in **13.4.5 Slave reception**	CHAPTER 13 SERIAL ARRAY UNIT
	Change of transfer rate in **13.4.6 Slave transmission/reception**	
	Change of **Note** in **13.4.7 (2)**	
	Addition of setting and **Note** to **Table 13-2 Selection of Operation Clock**	
	Change of transfer rate and addition of **Note**	
	Change of setting of **(e) Serial mode register mr (SMRmr)** in **Figure 13-74 Example of Contents of Registers for UART Reception of UART (UART0, UART1, UART2, UART3)**	
	Addition of setting and **Note** to **Table 13-3 Selection of Operation Clock**	
	Addition of setting and **Note** to **Table 13-4 Selection of Operation Clock**	
	Additions of description to **16.6 (4) DMA pending instruction**	CHAPTER 16 DMA CONTROLLER
	Change of **Figure 19-4 HALT Mode Release by Reset**	CHAPTER 19 STANDBY FUNCTION
	Change of **Figure 19-7 STOP Mode Release by Reset**	
	Change of reset processing in **Figure 20-2 Timing of Reset by $\overline{\text{RESET}}$ Input**	CHAPTER 20 RESET FUNCTION
	Change of reset processing in **Figure 20-4 Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input**	
	Change of **Caution 2** in **Figure 20-5 Format of Reset Control Flag Register (RESF)**	
	Change of **Figure 21-2 Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)**	CHAPTER 21 POWER-ON-CLEAR CIRCUIT
	Change of **Figure 21-2 Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)** and addition of **Note**	
	Change of **Figure 21-3 Example of Software Processing After Reset Release**	
	Change of **Note 4** in **Figure 22-2 Format of Low-Voltage Detection Register (LVIM)** and addition of **Caution 3**	CHAPTER 22 LOW-VOLTAGE DETECTOR
	Change of **Caution 2** in **Figure 22-3 Format of Low-Voltage Detection Level Select Register (LVIS)**	
	Change of <5> in **22.4.1 (1) (a)**	
	Change of **Note 2** in **Figure 22-5 Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)**	
	Change of description and **Caution** in **22.4.1 (1) (b)**	
	Change of **Figure 22-6 Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 0)** and **Note**	
	Change of <4> in **22.4.1 (2)**	
	Change of **Note 2** in **Figure 22-7 Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 1)**	
	Change of <5> in **22.4.2 (1)**	
	Additions of **Note 3** to **Figure 22-8 Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)**	
	Change of description and **Caution** in **22.4.2 (1) (b)**	
	Change of Figure 22-9 Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 0) and addition of Note	
	Change of <4> in 22.4.2 (2)	
	Addition of **Note 3** to **Figure 22-10 Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 1)**	
	Change of **Figure 22-11 Example of Software Processing After Reset Release**	