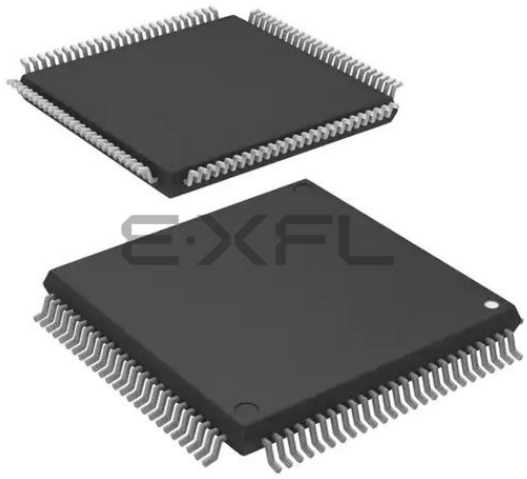
# Renesas Electronics America Inc - UPD78F1165AGF-GAS-AX Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

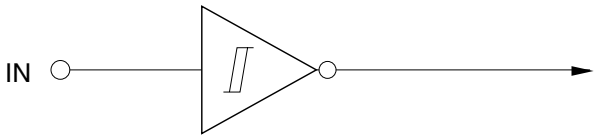
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0R |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | 3-Wire SIO, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 16x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1165agf-gas-ax |

## 1.6 78K0R/Kx3 Microcontroller Lineup

| ROM | RAM | 78K0R/KE3 | 78K0R/KF3 | 78K0R/KG3 | 78K0R/KH3 | 78K0R/KJ3 |
|---|---|---|---|---|---|---|
| | | 64 Pins | 80 Pins | 100 Pins | 128 Pins | 144 Pins |
| 512 KB | 30 KB | – | – | μPD78F1168 | μPD78F1178 | μPD78F1188A |
| | | | | μPD78F1168A | μPD78F1178A | |
| 384 KB | 24 KB | – | – | μPD78F1167 | μPD78F1177 | μPD78F1187A |
| | | | | μPD78F1167A | μPD78F1177A | |
| 256 KB | 12 KB | μPD78F1146 | μPD78F1156 | μPD78F1166 | μPD78F1176 | μPD78F1186A |
| | | μPD78F1146A | μPD78F1156A | μPD78F1166A | μPD78F1176A | |
| 192 KB | 10 KB | μPD78F1145 | μPD78F1155 | μPD78F1165 | μPD78F1175 | μPD78F1185A |
| | | μPD78F1145A | μPD78F1155A | μPD78F1165A | μPD78F1175A | |
| 128 KB | 8 KB | μPD78F1144 | μPD78F1154 | μPD78F1164 | μPD78F1174 | μPD78F1184A |
| | | μPD78F1144A | μPD78F1154A | μPD78F1164A | μPD78F1174A | |
| 96 KB | 6 KB | μPD78F1143 | μPD78F1153 | μPD78F1163 | – | – |
| | | μPD78F1143A | μPD78F1153A | μPD78F1163A | | |
| 64 KB | 4 KB | μPD78F1142 | μPD78F1152 | μPD78F1162 | – | – |
| | | μPD78F1142A | μPD78F1152A | μPD78F1162A | | |

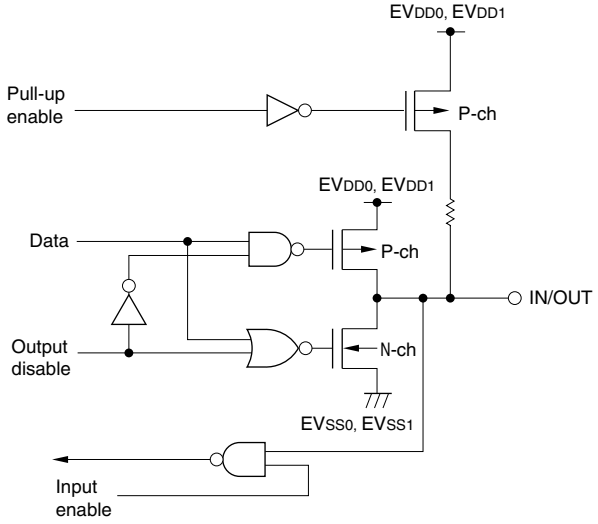
**Figure 2-1. Pin I/O Circuit List (1/2)**

Type 2

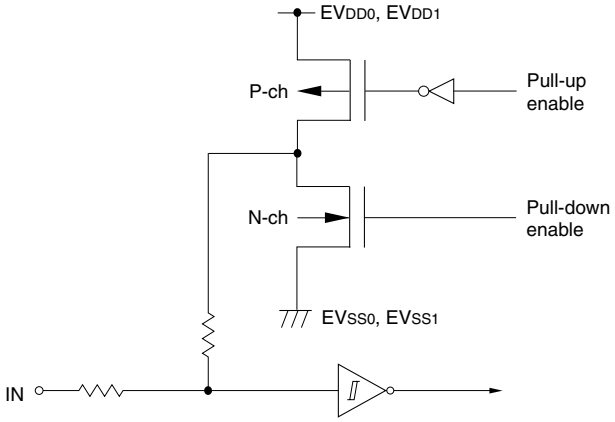



Schmitt-triggered input with hysteresis characteristics

Type 5-AG

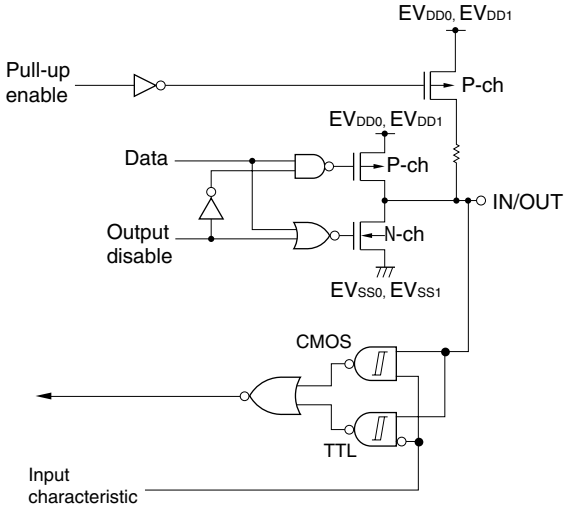



Type 2-W

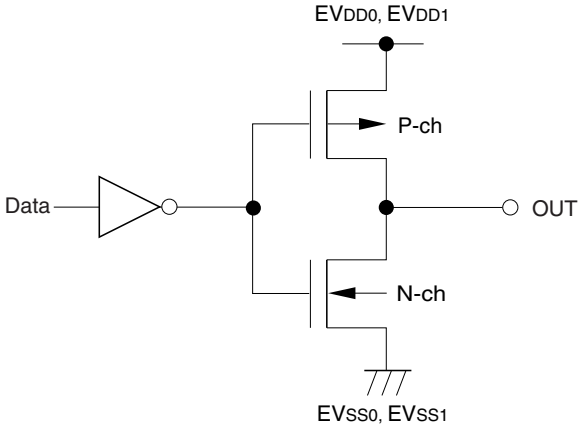



Schmitt-triggered input with hysteresis characteristics

Type 5-AN




Type 3-C




Type 8-R

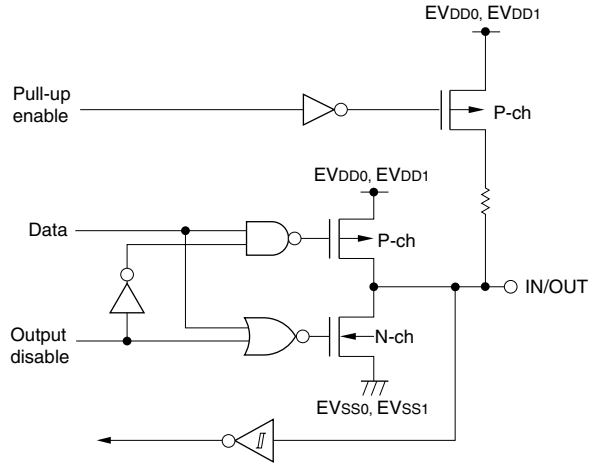
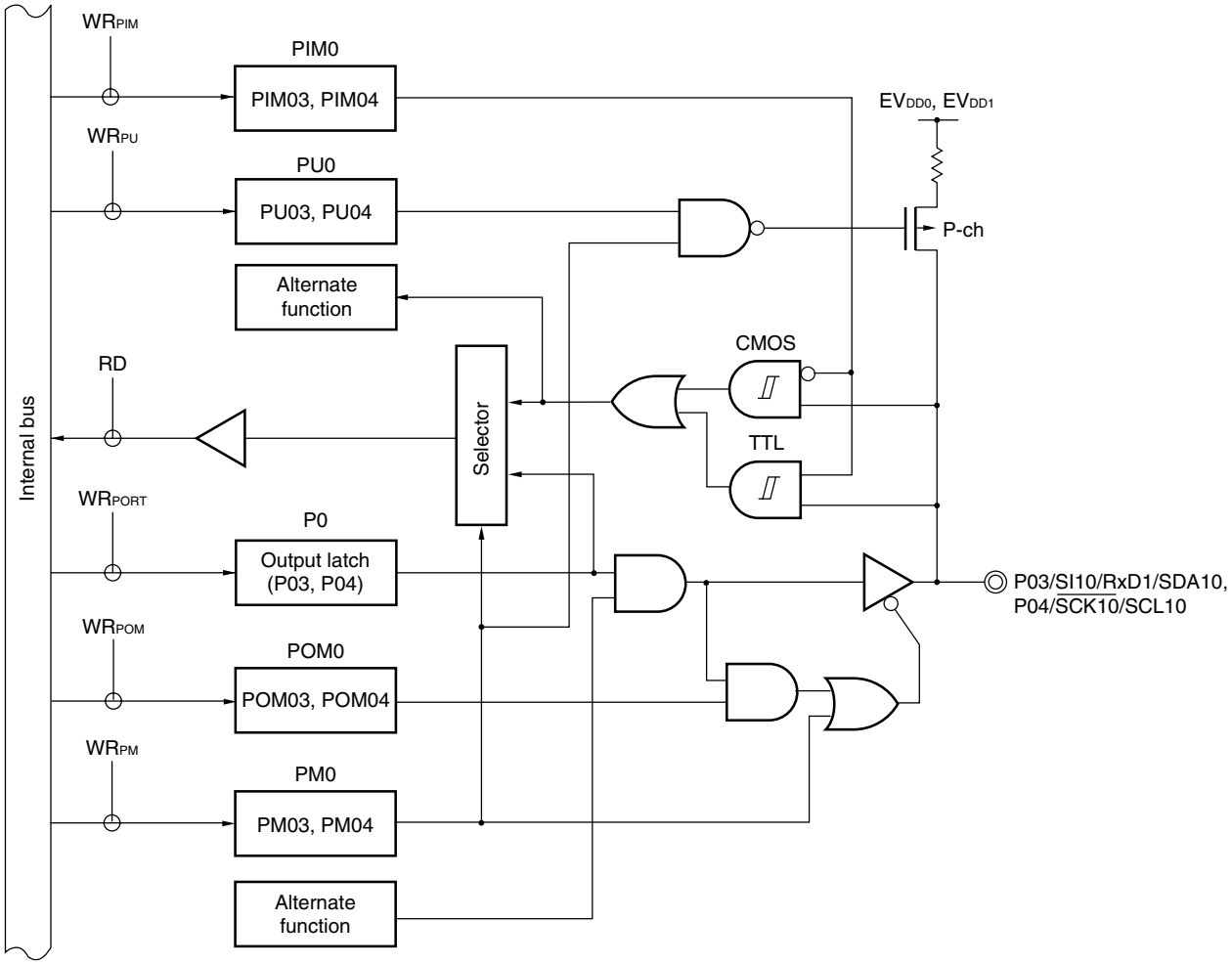
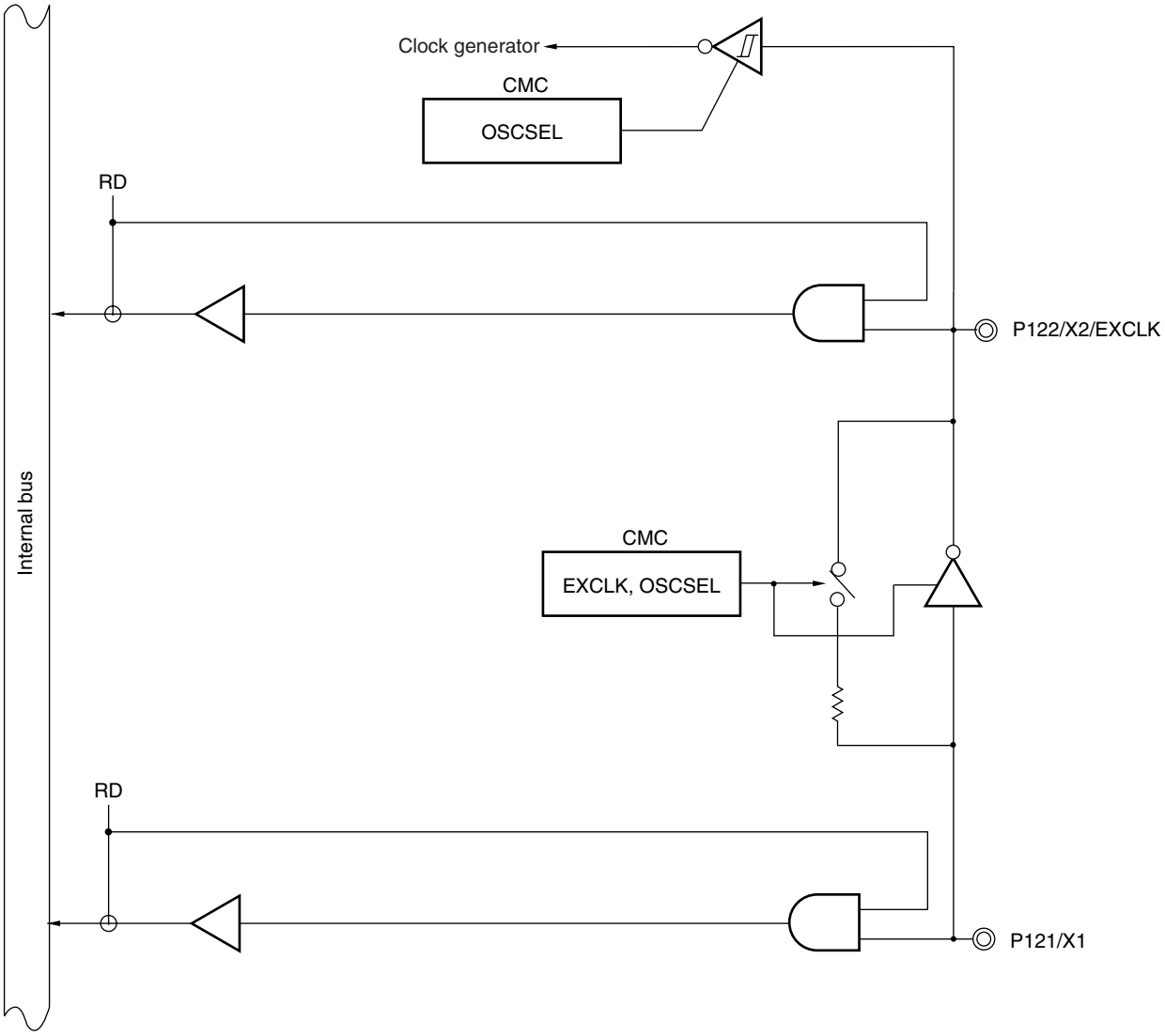


**Figure 4-5. Block Diagram of P03 and P04**




P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
PIM0: Port input mode register 0
POM0: Port output mode register 0
RD: Read signal
WR××: Write signal

**Figure 4-32. Block Diagram of P121 and P122**




CMC: Clock operation mode control register
RD: Read signal

**(2) Example of setting procedure when using the external main system clock**

<1> Setting P121/X1 and P122/X2/EXCLK pins (CMC register)

| EXCLK | OSCSEL | 0 | OSCSELS | 0 | 0 | 0 | AMPH |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0/1 | 0 | 0 | 0 | × |

**Remarks 1.** ×: don't care

**2.** For setting of the P123/XT1 and P124/XT2 pins, see **6.6.3 (1) Example of setting procedure when oscillating the subsystem clock**.

<2> Controlling external main system clock input (CSC register)

When MSTOP is cleared to 0, the input of the external main system clock is enabled.

**Cautions 1. The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction.**

**Therefore, it is necessary to also set the value of the OSCSELS bits at the same time. For OSCSELS bits, see 6.6.3 Example of controlling subsystem clock.**

**2. Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (see CHAPTER 29 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) and CHAPTER 30 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)).**

**(3) Example of setting procedure when using high-speed system clock as CPU/peripheral hardware clock**

<1> Setting high-speed system clock oscillation[Note]

(See **6.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

**Note** The setting of <1> is not necessary when high-speed system clock is already operating.

<2> Setting the high-speed system clock as the source clock of the CPU/peripheral hardware clock and setting the division ratio of the set clock (CKC register)

| MCM0 | MDIV2 | MDIV1 | MDIV0 | Selection of CPU/Peripheral Hardware Clock ($f_{CLK}$) |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | $f_{MX}$ |
| | 0 | 0 | 1 | $f_{MX}/2$ |
| | 0 | 1 | 0 | $f_{MX}/2^2$ |
| | 0 | 1 | 1 | $f_{MX}/2^3$ |
| | 1 | 0 | 0 | $f_{MX}/2^4$ |
| | 1 | 0 | 1 | $f_{MX}/2^5$ [Note] |

**Note** Setting is prohibited when $f_{MX}$ < 4 MHz.

**Figure 7-37. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (3/3)**

**(2) When $f_{SUB}$/4 is selected as count clock (continued)**

**(e) Timer output enable register 0 (TOE0)**

Bit n

| | | |
|---|---|---|
| TOE0 | TOE0n<br>1/0 | 0: Stops the TO0n output operation by counting operation.<br>1: Enables the TO0n output operation by counting operation. |

**(f) Timer output level register 0 (TOL0)**

Bit n

| | | |
|---|---|---|
| TOL0 | TOL0n<br>0 | 0: Cleared to 0 when TOM0n = 0 (toggle mode) |

**(g) Timer output mode register 0 (TOM0)**

Bit n

| | | |
|---|---|---|
| TOM0 | TOM0n<br>0 | 0: Sets toggle mode. |

**Remark** n = 0 to 7, m = 0, 1

## 7.8 Operation of Plural Channels of Timer Array Unit

### 7.8.1 Operation as PWM function

Two channels can be used as a set to generate a pulse of any period and duty factor.

The period and duty factor of the output pulse can be calculated by the following expressions.

| |
|---|
| Pulse period = {Set value of TDR0n (master) + 1} × Count clock period |
| Duty factor [%] = {Set value of TDR0m (slave)}/{Set value of TDR0n (master) + 1} × 100 |
| 0% output: Set value of TDR0m (slave) = 0000H |
| 100% output: Set value of TDR0m (slave) ≥ {Set value of TDR0n (master) + 1} |

**Remark** The duty factor exceeds 100% if the set value of TDR0m (slave) > (set value of TDR0n (master) + 1), it summarizes to 100% output.

The master channel operates in the interval timer mode and counts the periods. When the channel start trigger (TS0m) is set to 1, INTTM0n is output. TCR0n counts down starting from the loaded value of TDR0n, in synchronization with the count clock. When TCR0n = 0000H, INTTM0n is output. TCR0n loads the value of TDR0n again. After that, it continues the similar operation.

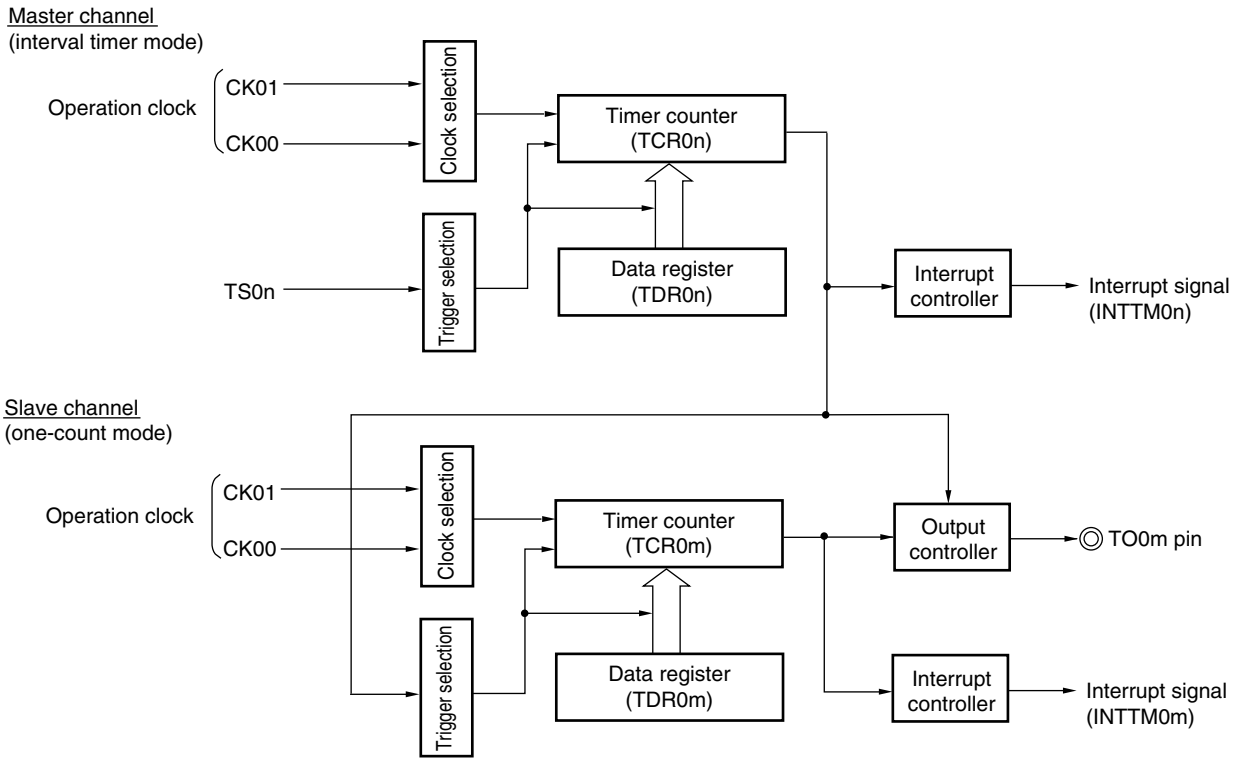
TCR0m of a slave channel operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TO0m pin. TCR0m of the slave channel loads the value of TDR0m, using INTTM0n of the master channel as a start trigger, and stops counting until the next start trigger (INTTM0n of the master channel) is input.

The output level of TO0m becomes active one count clock after generation of INTTM0n from the master channel, and inactive when TCR0m = 0000H.

**Caution To rewrite both TDR0n of the master channel and TDR0m of the slave channel, a write access is necessary two times. The timing at which the values of TDR0n and TDR0m are loaded to TCR0n and TRC0m is upon occurrence of INTTM0n of the master channel. Thus, when rewriting is performed split before and after occurrence of INTTM0n of the master channel, the TO0m pin cannot output the expected waveform. To rewrite both TDR0n of the master and TDR0m of the slave, therefore, be sure to rewrite both the registers immediately after INTTM0n is generated from the master channel.**

**Remark** n = 0, 2, 4, 6
m = n + 1

**Figure 7-55. Block Diagram of Operation as PWM Function**




**Remark** n = 0, 2, 4, 6
m = n + 1

**Figure 8-3. Format of Real-Time Counter Control Register 0 (RTCC0)**

Address: FFF9DH After reset: 00H R/W

| Symbol | <7> | 6 | <5> | <4> | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RTCC0 | RTCE | 0 | RCLOE1 | RCLOE0 | AMPM | CT2 | CT1 | CT0 |

| RTCE | Real-time counter operation control |
|---|---|
| 0 | Stops counter operation. |
| 1 | Starts counter operation. |

| RCLOE1 | RTC1HZ pin output control |
|---|---|
| 0 | Disables output of RTC1HZ pin (1 Hz). |
| 1 | Enables output of RTC1HZ pin (1 Hz). |

| RCLOE0[Note] | RTCCL pin output control |
|---|---|
| 0 | Disables output of RTCCL pin (32.768 kHz). |
| 1 | Enables output of RTCCL pin (32.768 kHz). |

| AMPM | Selection of 12-/24-hour system |
|---|---|
| 0 | 12-hour system (a.m. and p.m. are displayed.) |
| 1 | 24-hour system |
| Rewrite the AMPM value after setting RWAIT (bit 0 of RTCC1) to 1. If the AMPM value is changed, the values of the hour count register (HOUR) change according to the specified time system.<br>Table 8-2 shows the displayed time digits. | |

<R>

| CT2 | CT1 | CT0 | Constant-period interrupt (INTRTC) selection |
|---|---|---|---|
| 0 | 0 | 0 | Does not use constant-period interrupt function. |
| 0 | 0 | 1 | Once per 0.5 s (synchronized with second count up) |
| 0 | 1 | 0 | Once per 1 s (same time as second count up) |
| 0 | 1 | 1 | Once per 1 m (second 00 of every minute) |
| 1 | 0 | 0 | Once per 1 hour (minute 00 and second 00 of every hour) |
| 1 | 0 | 1 | Once per 1 day (hour 00, minute 00, and second 00 of every day) |
| 1 | 1 | × | Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month) |
| When changing the values of CT2 to CT0 while the counter operates (RTCE = 1), rewrite the values of CT2 to CT0 after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of CT2 to CT0, enable interrupt servicing after clearing the RIFG and RTCIF flags. | | | |

**Note** RCLOE0 and RCLOE2 must not be enabled at the same time.

**Caution If RCLOE0 and RCLOE1 are changed when RTCE = 1, glitches may occur in the 32.768 kHz and 1 Hz output signals.**

**Remark** ×: don't care

### (1) Register setting

**Figure 13-56. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20)**

**(a) Serial output register m (SOm) …The register that not used in this mode.**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOm | 0 | 0 | 0 | 0 | 1 | CKOm2 × | CKOm1 × | CKOm0 × | 0 | 0 | 0 | 0 | 1 | SOm2 × | SOm1 × | SOm0 × |

<R> **(b) Serial output enable register m (SOEm) …The register that not used in this mode.**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOEm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm2 × | SOEm1 × | SOEm0 × |

**(c) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SSm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm3 × | SSm2 0/1 | SSm1 0/1 | SSm0 0/1 |

**(d) Serial mode register mn (SMRmn)**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SMRmn | CKSmn 0/1 | CCSmn 1 | 0 | 0 | 0 | 0 | 0 | STSmn 0 | 0 | SISmn0 0 | 1 | 0 | 0 | MDmn2 0 | MDmn1 0 | MDmn0 0 |

Interrupt sources of channel n
0: Transfer end interrupt

**(e) Serial communication operation setting register mn (SCRmn)**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SCRmn | TXEmn 0 | RXEmn 1 | DAPmn 0/1 | CKPmn 0/1 | 0 | EOCmn 0 | PTCmn1 0 | PTCmn0 0 | DIRmn 0/1 | 0 | SLCmn1 0 | SLCmn0 0 | 0 | DLSmn2 1 | DLSmn1 1 | DLSmn0 0/1 |

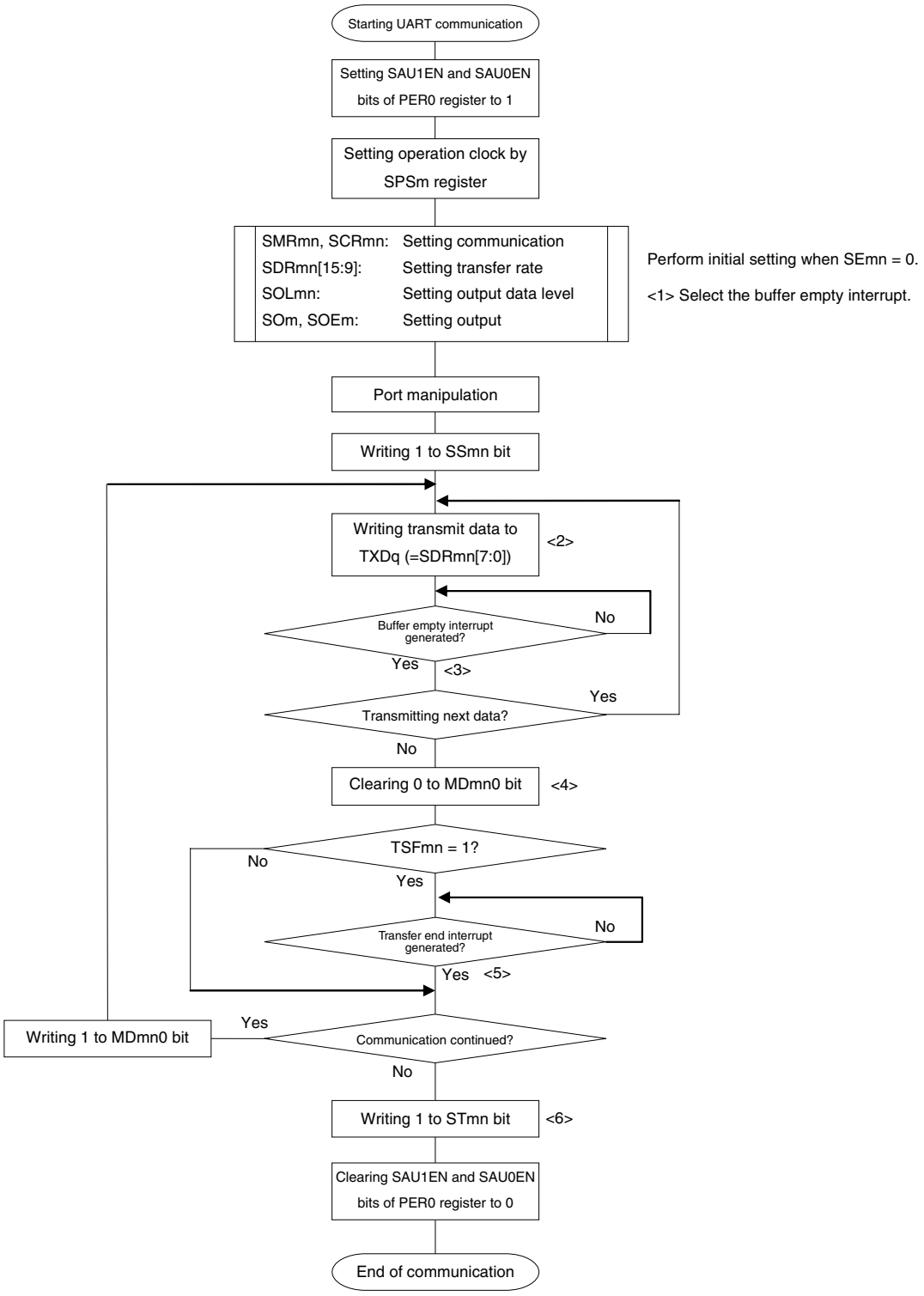
**(f) Serial data register mn (SDRmn) (lower 8 bits: SIOp)**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SDRmn | 0000000 (baud rate setting) | | | | | | | 0 | Receive data register | | | | | | | |

SIOp

**Remark** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20)
□: Setting is fixed in the CSI slave reception mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

**Figure 13-78. Flowchart of UART Transmission (in Continuous Transmission Mode)**




**Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.**

**Remark** <1> to <6> in the figure correspond to <1> to <6> in **Figure 13-77 Timing Chart of UART Transmission (in Continuous Transmission Mode)**.

**Table 13-3. Selection of Operation Clock**

| SMRmn Register | SPSm Register | | | | | | | | Operation Clock (MCK)[Note 1] | |
|---|---|---|---|---|---|---|---|---|---|---|
| CKSmn | PRS m13 | PRS m12 | PRS m11 | PRS m10 | PRS m03 | PRS m02 | PRS m01 | PRS m00 | | $f_{CLK}$ = 20 MHz |
| 0 | X | X | X | X | 0 | 0 | 0 | 0 | $f_{CLK}$ | 20 MHz |
| | X | X | X | X | 0 | 0 | 0 | 1 | $f_{CLK}/2$ | 10 MHz |
| | X | X | X | X | 0 | 0 | 1 | 0 | $f_{CLK}/2^2$ | 5 MHz |
| | X | X | X | X | 0 | 0 | 1 | 1 | $f_{CLK}/2^3$ | 2.5 MHz |
| | X | X | X | X | 0 | 1 | 0 | 0 | $f_{CLK}/2^4$ | 1.25 MHz |
| | X | X | X | X | 0 | 1 | 0 | 1 | $f_{CLK}/2^5$ | 625 kHz |
| | X | X | X | X | 0 | 1 | 1 | 0 | $f_{CLK}/2^6$ | 313 kHz |
| | X | X | X | X | 0 | 1 | 1 | 1 | $f_{CLK}/2^7$ | 156 kHz |
| | X | X | X | X | 1 | 0 | 0 | 0 | $f_{CLK}/2^8$ | 78.1 kHz |
| | X | X | X | X | 1 | 0 | 0 | 1 | $f_{CLK}/2^9$ | 39.1 kHz |
| | X | X | X | X | 1 | 0 | 1 | 0 | $f_{CLK}/2^{10}$ | 19.5 kHz |
| | X | X | X | X | 1 | 0 | 1 | 1 | $f_{CLK}/2^{11}$ | 9.77 kHz |
| | X | X | X | X | 1 | 1 | 1 | 1 | INTTM02 if m = 0, INTTM03 if m = 1[Note 2] | |
| 1 | 0 | 0 | 0 | 0 | X | X | X | X | $f_{CLK}$ | 20 MHz |
| | 0 | 0 | 0 | 1 | X | X | X | X | $f_{CLK}/2$ | 10 MHz |
| | 0 | 0 | 1 | 0 | X | X | X | X | $f_{CLK}/2^2$ | 5 MHz |
| | 0 | 0 | 1 | 1 | X | X | X | X | $f_{CLK}/2^3$ | 2.5 MHz |
| | 0 | 1 | 0 | 0 | X | X | X | X | $f_{CLK}/2^4$ | 1.25 MHz |
| | 0 | 1 | 0 | 1 | X | X | X | X | $f_{CLK}/2^5$ | 625 kHz |
| | 0 | 1 | 1 | 0 | X | X | X | X | $f_{CLK}/2^6$ | 313 kHz |
| | 0 | 1 | 1 | 1 | X | X | X | X | $f_{CLK}/2^7$ | 156 kHz |
| | 1 | 0 | 0 | 0 | X | X | X | X | $f_{CLK}/2^8$ | 78.1 kHz |
| | 1 | 0 | 0 | 1 | X | X | X | X | $f_{CLK}/2^9$ | 39.1 kHz |
| | 1 | 0 | 1 | 0 | X | X | X | X | $f_{CLK}/2^{10}$ | 19.5 kHz |
| | 1 | 0 | 1 | 1 | X | X | X | X | $f_{CLK}/2^{11}$ | 9.77 kHz |
| | 1 | 1 | 1 | 1 | X | X | X | X | INTTM02 if m = 0, INTTM03 if m = 1[Note 2] | |
| Other than above | | | | | | | | | Setting prohibited | |

**Notes 1.** When changing the clock selected for $f_{CLK}$ (by changing the system clock control register (CKC) value), do so after having stopped (STm = 000FH) the operation of the serial array unit (SAU). When selecting INTTM02 and INTTM03 for the operation clock, also stop the timer array unit (TAU) (TT0 = 00FFH).

**2.** SAU can be operated at a fixed division ratio of the subsystem clock, regardless of the $f_{CLK}$ frequency (main system clock, subsystem clock), by operating the interval timer for which $f_{SUB}/4$ has been selected as the count clock (setting TIS02 (if m = 0) or TIS03 (if m = 1) of the TIS0 register to 1) and selecting INTTM02 and INTTM03 by using the SPSm register in channels 2 and 3 of TAU. When changing $f_{CLK}$, however, SAU and TAU must be stopped as described in Note 1 above.

**Remarks 1.** X: Don't care

**2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

### 14.5.9 Interrupt request (INTIIC0) generation timing and wait control

The setting of bit 3 (WTIM0) of IIC control register 0 (IICC0) determines the timing by which INTIIC0 is generated and the corresponding wait control, as shown in Table 14-4.

**Table 14-4. INTIIC0 Generation Timing and Wait Control**

| WTIM0 | During Slave Device Operation | | | During Master Device Operation | | |
|---|---|---|---|---|---|---|
| | Address | Data Reception | Data Transmission | Address | Data Reception | Data Transmission |
| 0 | 9 Notes 1, 2 | 8 Note 2 | 8 Note 2 | 9 | 8 | 8 |
| 1 | 9 Notes 1, 2 | 9 Note 2 | 9 Note 2 | 9 | 9 | 9 |

**Notes 1.** The slave device's INTIIC0 signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to slave address register 0 (SVA0).
At this point, $\overline{ACK}$ is generated regardless of the value set to IICC0's bit 2 (ACKE0). For a slave device that has received an extension code, INTIIC0 occurs at the falling edge of the eighth clock.
However, if the address does not match after restart, INTIIC0 is generated at the falling edge of the 9th clock, but wait does not occur.

**2.** If the received address does not match the contents of slave address register 0 (SVA0) and extension code is not received, neither INTIIC0 nor a wait occurs.

**Remark** The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

**(1) During address transmission/reception**

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

**(2) During data reception**

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

**(3) During data transmission**

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

**(4) Wait cancellation method**

The four wait cancellation methods are as follows.

- Writing data to IIC shift register 0 (IIC0)
- Setting bit 5 (WREL0) of IIC control register 0 (IICC0) (canceling wait)
- Setting bit 1 (STT0) of IIC0 register (generating start condition) Note
- Setting bit 0 (SPT0) of IIC0 register (generating stop condition) Note

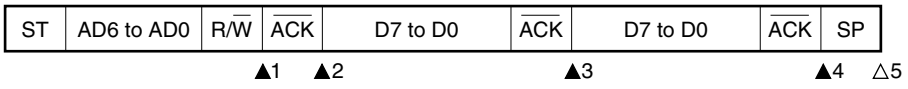
**Note** Master only.

When an 8-clock wait has been selected (WTIM0 = 0), the presence/absence of $\overline{ACK}$ generation must be determined prior to wait cancellation.

**(5) Stop condition detection**

INTIIC0 is generated when a stop condition is detected (only when SPIE0 = 1).

**(ii) When WTIM0 = 1**



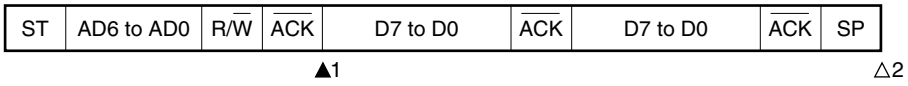

▲1: IICS0 = 0110×010B
▲2: IICS0 = 0010×110B
▲3: IICS0 = 0010×100B
▲4: IICS0 = 0010××00B
△5: IICS0 = 00000001B

**Remark** ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

**(6) Operation when arbitration loss occurs (no communication after arbitration loss)**

When the device is used as a master in a multi-master system, read the MSTS0 bit each time interrupt request signal INTIIC0 has occurred to check the arbitration result.

**(a) When arbitration loss occurs during transmission of slave address data (when WTIM0 = 1)**




▲1: IICS0 = 01000110B
△2: IICS0 = 00000001B

**Remark** ▲: Always generated
△: Generated only when SPIE0 = 1

**Table 17-1. Interrupt Source List (1/2)**

| Interrupt Type | Default Priority[Note 1] | Interrupt Source | | Internal/ External | Vector Table Address | Basic Configuration Type[Note 2] |
|---|---|---|---|---|---|---|
| | | Name | Trigger | | | |
| Maskable | 0 | INTWDTI | Watchdog timer interval[Note 3] (75% of overflow time) | Internal | 0004H | (A) |
| | 1 | INTLVI | Low-voltage detection[Note 4] | | 0006H | |
| | 2 | INTP0 | Pin input edge detection | External | 0008H | (B) |
| | 3 | INTP1 | | | 000AH | |
| | 4 | INTP2 | | | 000CH | |
| | 5 | INTP3 | | | 000EH | |
| | 6 | INTP4 | | | 0010H | |
| | 7 | INTP5 | | | 0012H | |
| | 8 | INTST3 | UART3 transmission transfer end or buffer empty interrupt | Internal | 0014H | (A) |
| | 9 | INTSR3 | UART3 reception transfer end | | 0016H | |
| | 10 | INTSRE3 | UART3 reception communication error occurrence | | 0018H | |
| | 11 | INTDMA0 | End of DMA0 transfer | | 001AH | |
| | 12 | INTDMA1 | End of DMA1 transfer | | 001CH | |
| | 13 | INTST0 /INTCSI00 | UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt | | 001EH | |
| | 14 | INTSR0 /INTCSI01 | UART0 reception transfer end/ CSI01 transfer end or buffer empty interrupt | | 0020H | |
| | 15 | INTSRE0 | UART0 reception communication error occurrence | | 0022H | |
| | 16 | INTST1 /INTCSI10 /INTIIC10 | UART1 transmission transfer end or buffer empty interrupt/ CSI10 transfer end or buffer empty interrupt/ IIC10 transfer end | | 0024H | |
| | 17 | INTSR1 | UART1 reception transfer end | | 0026H | |
| | 18 | INTSRE1 | UART1 reception communication error occurrence | | 0028H | |
| | 19 | INTIIC0 | End of IIC0 communication | | 002AH | |
| | 20 | INTTM00 | End of timer channel 0 count or capture | | 002CH | |
| | 21 | INTTM01 | End of timer channel 1 count or capture | | 002EH | |
| | 22 | INTTM02 | End of timer channel 2 count or capture | | 0030H | |
| | 23 | INTTM03 | End of timer channel 3 count or capture | | 0032H | |

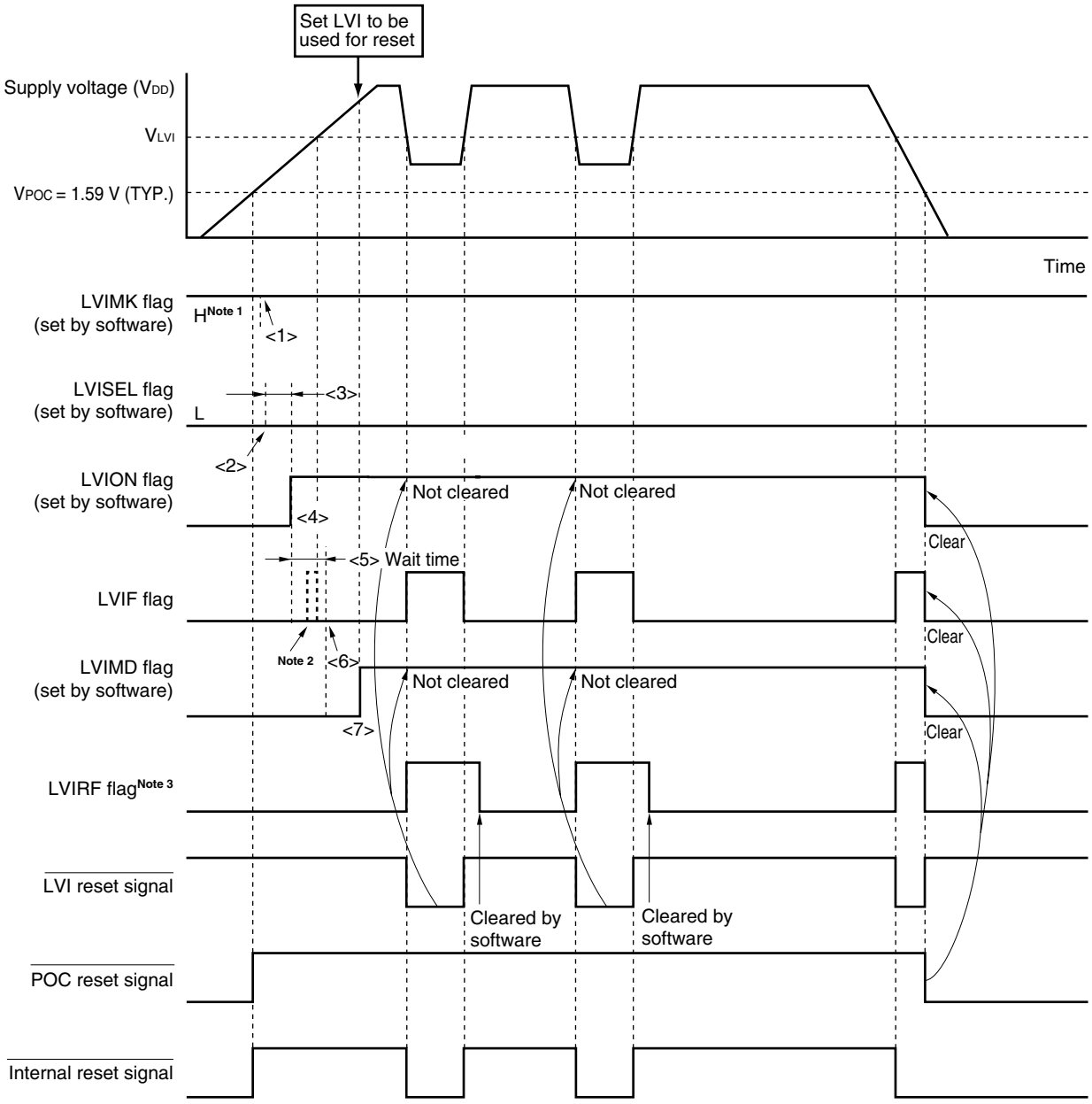
**Notes 1.** The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.

**2.** Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 17-1.

**3.** When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

**4.** When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

**Figure 22-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)**




**Notes 1.** The LVIMK flag is set to “1” by reset signal generation.

**2.** The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

**3.** LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 20 RESET FUNCTION**.

**Remark** <1> to <7> in Figure 22-5 above correspond to <1> to <7> in the description of “When starting operation” in **22.4.1 (1) (a) When LVI default start function stopped is set (option byte: LVIOFF = 1).**

# CHAPTER 29 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)

Target products Conventional-specification products: μPD78F1162, 78F1163, 78F1164, 78F1165, 78F1166, 78F1167, 78F1168

Expanded-specification products: μPD78F1162A, 78F1163A, 78F1164A, 78F1165A, 78F1166A, 78F1167A, 78F1168A

**Caution The 78K0R/KG3 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. NEC Electronics is not liable for problems occurring when the on-chip debug function is used.**

## Absolute Maximum Ratings ($T_A$ = 25°C) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | −0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0} = EV_{DD1}$ | −0.5 to +6.5 | V |
| | $V_{SS}$ | | −0.5 to +0.3 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0} = EV_{SS1}$ | −0.5 to +0.3 | V |
| | $AV_{REF0}$ | | −0.5 to $V_{DD}$ + 0.3 Note 1 | V |
| | $AV_{REF1}$ | | −0.5 to $V_{DD}$ + 0.3 Note 1 | V |
| | $AV_{SS}$ | | −0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | −0.3 to +3.6 and −0.3 to $V_{DD}$ + 0.3 Note 2 | V |
| Input voltage | $V_{I1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P120 to P124, P131, P140 to P145, EXCLK, $\overline{\text{RESET}}$, FLMD0 | −0.3 to $EV_{DD0}$, $EV_{DD1}$ + 0.3 and −0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | −0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P150 to P157 | −0.3 to $AV_{REF0}$ + 0.3 and −0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| | $V_{I4}$ | P110, P111 | −0.3 to $AV_{REF1}$ + 0.3 and −0.3 to $V_{DD}$ + 0.3 Note 1 | V |
| Output voltage | $V_{O1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P120, P130, P131, P140 to P145 | −0.3 to $EV_{DD0}$, $EV_{DD1}$ + 0.3 Note 1 | V |
| | $V_{O2}$ | P20 to P27, P150 to P157 | −0.3 to $AV_{REF0}$ + 0.3 | V |
| | $V_{O3}$ | P110, P111 | −0.3 to $AV_{REF1}$ + 0.3 | V |

**Notes 1.** Must be 6.5 V or lower.

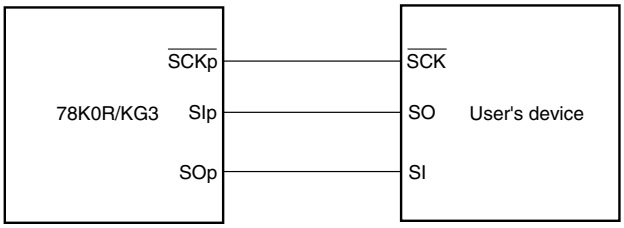
**2.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

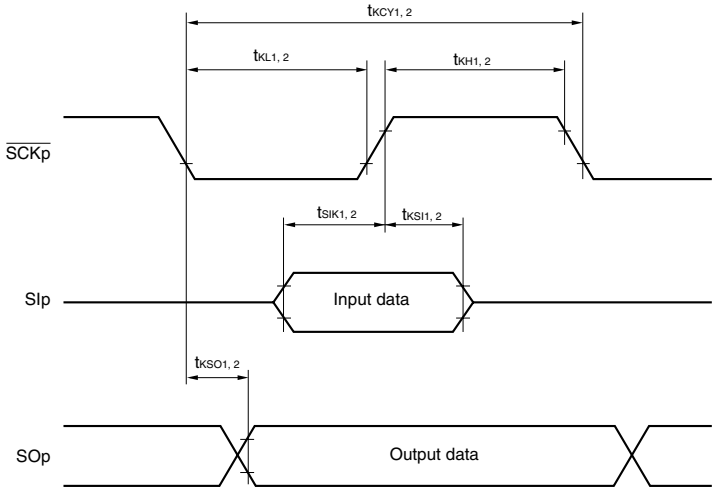
**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**(3) Serial interface: Serial array unit (4/18)**

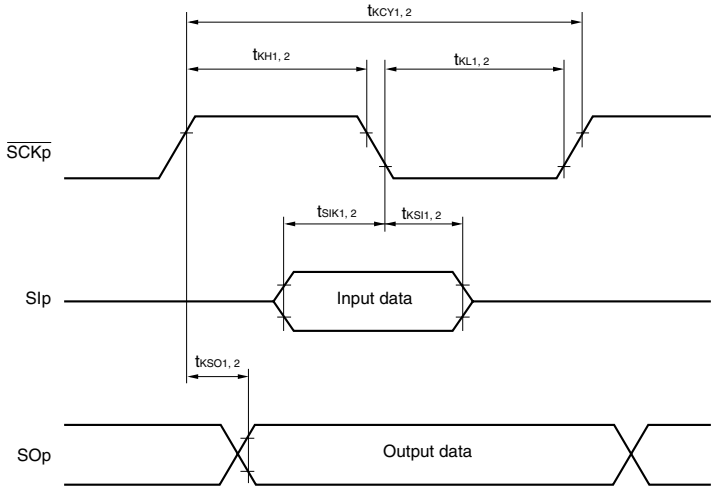
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)**

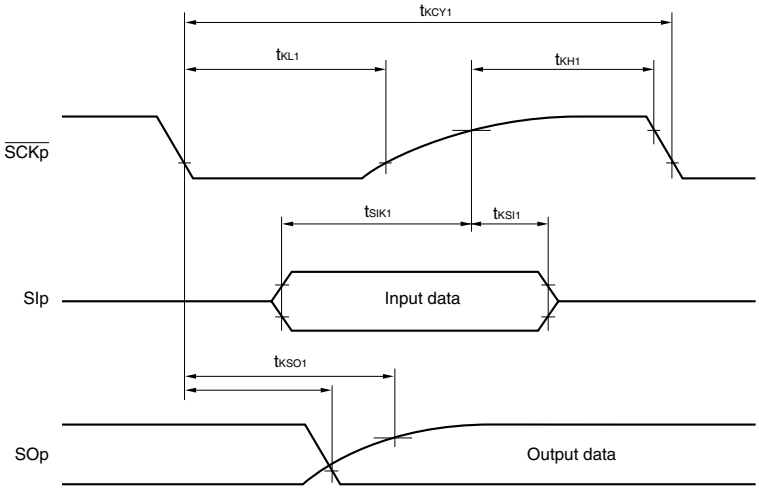



**Remarks 1.** p: CSI number (p = 00, 01, 10, 20)

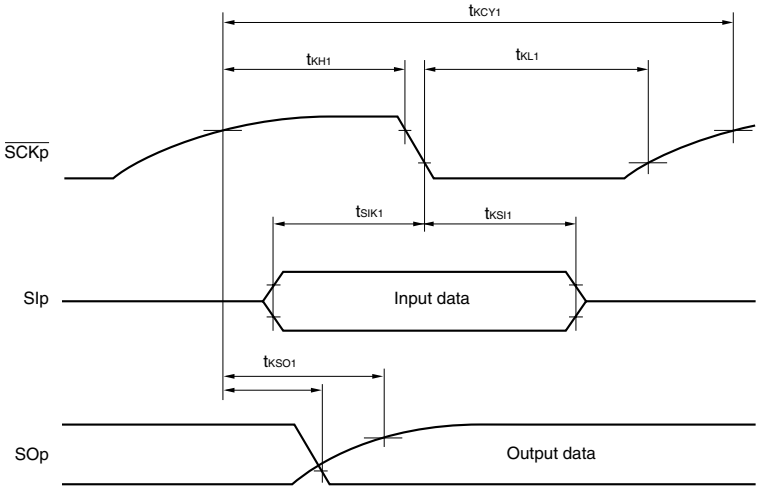
**2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

**(3) Serial interface: Serial array unit (13/18)**

**CSI mode serial transfer timing (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**




**CSI mode serial transfer timing (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)**




**Caution Select the TTL input buffer for SIp and the N-ch open-drain output ($V_{DD}$ tolerance) mode for SOp and $\overline{\text{SCKp}}$ by using the PIMg and POMg registers.**

**Remarks 1.** p: CSI number (p = 01, 10, 20), g: PIM and POM number (g = 0, 4, 14)

**2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

**3.** CSI00 cannot communicate at different potential. Use CSI01, CSI10, and CSI20 for communication at different potential.

(5/24)

| Edition | Description | Chapter |
|---|---|---|
| 3rd edition | Deletion of descriptions of CALLF instruction in **CHAPTER 3** | CHAPTER 3 CPU ARCHITECTURE |
| | Modification of description in **3.1 Memory Space** | |
| | Addition of **Note** in **Figure 3-5 Memory Map (μPD78F1166)** and **Figure 3-13 Correspondence Between Data Memory and Addressing (μPD78F1166)** | |
| | Addition of **Note** in **Figure 3-7 Memory Map (μPD78F1168)** and **Figure 3-15 Correspondence Between Data Memory and Addressing (μPD78F1168)** | |
| | Modification of description and addition of diagram example and explanation of PMC register in **3.1.2 Mirror area** | |
| | Change of reset value of Hour count register and Alarm hour register in **Table 3-5 SFR List** | |
| | Change of reset value of Day count register and Month count register in **Table 3-5 SFR List** | |
| | Change of reset value of Back ground event control register in **Table 3-5 SFR List** | |
| | Addition of BCD correction carry register and **Note** to **Table 3-5 SFR List** | |
| | Change of symbols of higher multiplication result storage register and lower multiplication result storage register in **Table 3-5 SFR List** | |
| | Addition of Regulator mode control register and BCD adjust result register in **Table 3-6 Extended SFR (2nd SFR) List** | |
| | Addition of SFR name for the lower 8 bits and modifications of R/W attribute and manipulable bit range for registers SSRmn, SIRmn, SEm, SSm, STm, SPSm, SOEm, SOLm, TCR0n, TSR0n, TE0, TS0, TT0, TPS0, TO0, TOE0, TOL0, and TOM0 in **Table 3-6 Extended SFR (2nd SFR) List** | |
| | Change of reset value of Serial output register 0 and Serial output register 1 in **Table 3-6 Extended SFR (2nd SFR) List** | |
| | Change of reset value of Serial output enable register 0 and Serial output enable register 1 in **Table 3-6 Extended SFR (2nd SFR) List** | |
| | Change of R/W attribute of Timer channel counter register 0n in **Table 3-6 Extended SFR (2nd SFR) List** | |
| | Addition of **3.3 Instruction Address Addressing** | |
| | Addition of **3.4 Addressing for Processing Data Addresses** | |
| | Addition of **Cautions 1** and **2** to **4.2.1 Port 0** | CHAPTER 4 PORT FUNCTIONS |
| | Addition of **Cautions 1** and **2** to **4.2.2 Port 1** | |
| | Addition of **Caution** to **4.2.4 Port 3** | |
| | Addition of **Cautions 2** and **3** to **4.2.5 Port 4** | |
| | Modification of **Figure 4-28 Block Diagram of P80 to P87** and **Figure 4-29 Block Diagram of P110 and P111** | |
| | Addition of **Caution** to **4.2.12 Port 13** | |
| | Addition of **Cautions 1** and **2** to **4.2.13 Port 14** | |
| | Addition of **Caution** to **Figure 4-39 Format of Port Mode Register** | |
| | Modification of **Note** in **4.3 (2) Port registers (P0 to P8, P11 to P15)** | |
| | Addition of **4.4.4 Connecting to external device with different power supply voltage (3 V)** | |
| | Addition of **Note** to **Figure 5-3 Format of Memory Extension Mode Control Register (MEM)** | CHAPTER 5 EXTERNAL BUS INTERFACE |
| | Modification of description in **5.6 (5) ASTB pin** and **(6) EX0 to EX7, EX8 to EX15, EX16 to EX23, and EX24 to EX31 pins** | |
| | Modification of **Figure 5-9 Example of Synchronous Memory Connection** and **Figure 5-10 Example of Asynchronous Memory Connection** | |