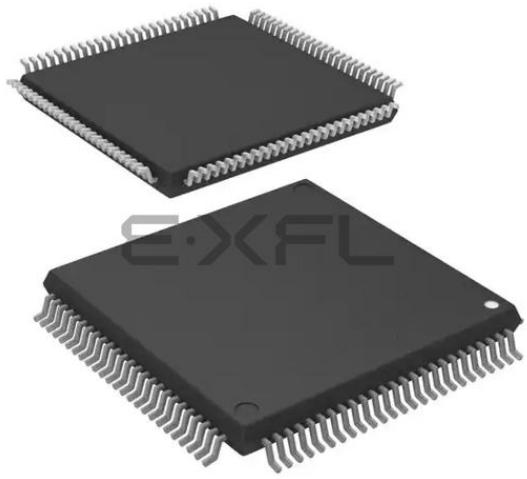
Renesas Electronics America Inc - UPD78F1167AGC-UEU-AX Datasheet



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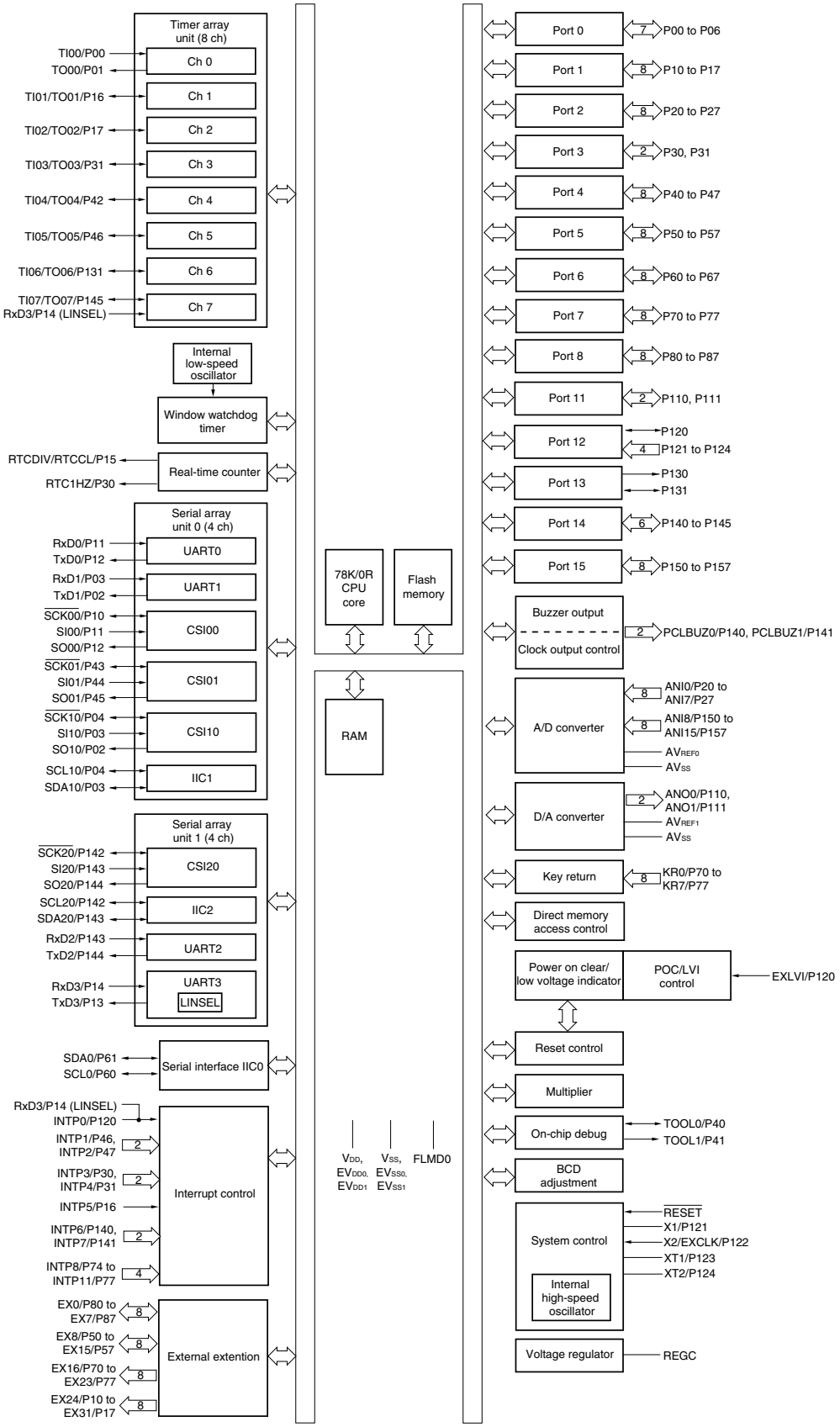
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1167agc-ueu-ax

1.7 Block Diagram



3.1.4 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FFF00H to FFFFFH (see **Table 3-5** in **3.2.4 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

3.1.5 Extended special function register (2nd SFR: 2nd Special Function Register) area

On-chip peripheral hardware special function registers (2nd SFRs) are allocated in the area F0000H to F07FFH (see **Table 3-6** in **3.2.5 Extended Special function registers (2nd SFRs: 2nd Special Function Registers)**).

SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Caution Do not access addresses to which the 2nd SFR is not assigned.

Table 3-5. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF90H	Sub-count register	RSUBC	R	–	–	√	0000H
FFF91H							
FFF92H	Second count register	SEC	R/W	–	√	–	00H
FFF93H	Minute count register	MIN	R/W	–	√	–	00H
FFF94H	Hour count register	HOUR	R/W	–	√	–	12H[Note 1]
FFF95H	Week count register	WEEK	R/W	–	√	–	00H
FFF96H	Day count register	DAY	R/W	–	√	–	01H
FFF97H	Month count register	MONTH	R/W	–	√	–	01H
FFF98H	Year count register	YEAR	R/W	–	√	–	00H
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H
FFF9AH	Alarm minute register	ALARMWM	R/W	–	√	–	00H
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	12H
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	00H
FFF9DH	Real-time counter control register 0	RTCC0	R/W	√	√	–	00H
FFF9EH	Real-time counter control register 1	RTCC1	R/W	√	√	–	00H
FFF9FH	Real-time counter control register 2	RTCC2	R/W	√	√	–	00H
FFFA0H	Clock operation mode control register	CMC	R/W	–	√	–	00H
FFFA1H	Clock operation status control register	CSC	R/W	√	√	–	C0H
FFFA2H	Oscillation stabilization time counter status register	OSTC	R	√	√	–	00H
FFFA3H	Oscillation stabilization time select register	OSTS	R/W	–	√	–	07H
FFFA4H	System clock control register	CKC	R/W	√	√	–	09H
FFFA5H	Clock output select register 0	CKS0	R/W	√	√	–	00H
FFFA6H	Clock output select register 1	CKS1	R/W	√	√	–	00H
FFFA8H	Reset control flag register	RESF	R	–	√	–	00H[Note 2]
FFFA9H	Low-voltage detection register	LVIM	R/W	√	√	–	00H[Note 3]
FFFAAH	Low-voltage detection level select register	LVIS	R/W	√	√	–	0EH[Note 4]
FFFABH	Watchdog timer enable register	WDTE	R/W	–	√	–	1A/9A[Note 5]
FFFACH	–	TTBLH[Note 6]	–	–	–	–	Undefined
FFFADH							
FFFAEH	–	TTBLL[Note 6]	–	–	–	–	Undefined
FFFAFH							

Notes 1. The value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

2. The reset value of RESF varies depending on the reset source.

3. The reset value of LVIM varies depending on the reset source and the setting of the option byte.

4. The reset value of LVIS varies depending on the reset source.

5. The reset value of WDTE is determined by the setting of the option byte.

6. Do not directly operate this SFR, because it cannot be used by the user.

Figure 4-41. Format of Port Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	P06	P05	P04	P03	P02	P01	P00	FFF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	0	P31	P30	FFF03H	00H (output latch)	R/W
P4	P47	P46	P45	P44	P43	P42	P41	P40	FFF04H	00H (output latch)	R/W
P5	P57	P56	P55	P54	P53	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	P67	P66	P65	P64	P63	P62	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	P87	P86	P85	P84	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P11	0	0	0	0	0	0	P111	P110	FFF0BH	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P13	0	0	0	0	0	0	P131	P130	FFF0DH	00H (output latch)	R/W
P14	0	0	P145	P144	P143	P142	P141	P140	FFF0EH	00H (output latch)	R/W
P15	P157	P156	P155	P154	P153	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 8, 11 to 15; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124 are read-only.

4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register and output latch as shown in Table 4-6.

Table 4-6. Settings of Port Mode Register and Output Latch When Using Alternate Function (1/3)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P00	TI00	Input	1	×
P01	TO00	Output	0	0
P02	SO10	Output	0	1
	TxD1	Output	0	1
P03	SI10	Input	1	×
	RxD1	Input	1	×
	SDA10	I/O	0	1
P04	$\overline{\text{SCK10}}$	Input	1	×
		Output	0	1
	SCL10	I/O	0	1
P05	CLKOUT	Output	0	0
P06	$\overline{\text{WAIT}}$	Input	1	×
P10	$\overline{\text{SCK00}}$	Input	1	×
		Output	0	1
	EX24	Output	0	0
P11	SI00	Input	1	×
	RxD0	Input	1	×
	EX25	Output	0	0
P12	SO00	Output	0	1
	TxD0	Output	0	1
	EX26	Output	0	0
P13	TxD3	Output	0	1
	EX27	Output	0	0
P14	RxD3	Input	1	×
	EX28	Output	0	0
P15	RTCDIV	Output	0	0
	RTCCL	Output	0	0
	EX29	Output	0	0
P16	TI01	Input	1	×
	TO01	Output	0	0
	INTP5	Input	1	×
	EX30	Output	0	0

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

4.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0R/KG3.

<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-46. Bit Manipulation Instruction (P10)

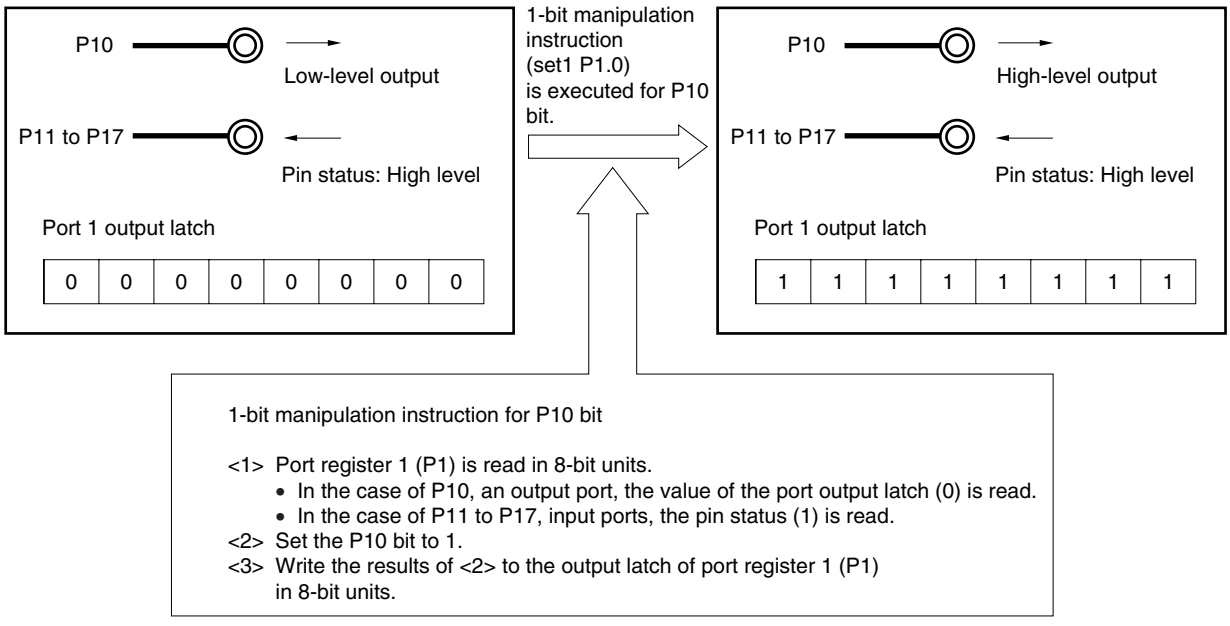


Figure 6-7. Format of Peripheral Enable Register (2/2)

SAU1EN	Control of serial array unit 1 input clock
0	Stops input clock supply. • SFR used by the serial array unit 1 cannot be written. • The serial array unit 1 is in the reset status.
1	Supplies input clock. • SFR used by the serial array unit 1 can be read and written.

SAU0EN	Control of serial array unit 0 input clock
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Supplies input clock. • SFR used by the serial array unit 0 can be read and written.

TAU0EN	Control of timer array unit input clock
0	Stops input clock supply. • SFR used by the timer array unit cannot be written. • The timer array unit is in the reset status.
1	Supplies input clock. • SFR used by the timer array unit can be read and written.

EXBEN	Control of external bus interface input clock
0	Stops input clock supply. • SFR used by the external bus interface cannot be written. • The external bus interface is in the reset status.
1	Supplies input clock. • SFR used by the external bus interface can be read and written.

Caution Be sure to clear bit 1 of the PER0 register and bits 1 to 7 of the PER1 register to 0.

7.7.3 Operation as frequency divider (channel 0 only)

The timer array unit can be used as a frequency divider that divides a clock input to the TI00 pin and outputs the result from TO00.

The divided clock frequency output from TO00 can be calculated by the following expression.

- When rising edge/falling edge is selected:
  Divided clock frequency = Input clock frequency/{(Set value of TDR00 + 1) × 2}
- When both edges are selected:
  Divided clock frequency ≅ Input clock frequency/(Set value of TDR00 + 1)

TCR00 operates as a down counter in the interval timer mode.

After the channel start trigger bit (TS00) is set to 1, TCR00 loads the value of TDR00 when the TI00 valid edge is detected. If MD000 of TMR00 = 0 at this time, INTTM00 is not output and TO00 is not toggled. If MD000 of TMR00 = 1, INTTM00 is output and TO00 is toggled.

After that, TCR00 counts down at the valid edge of TI00. When TCR00 = 0000H, it toggles TO00. At the same time, TCR00 loads the value of TDR00 again, and continues counting.

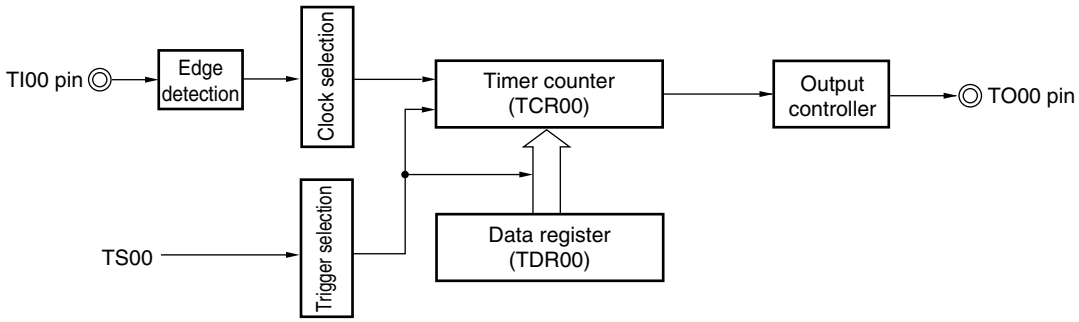
If detection of both the edges of TI00 is selected, the duty factor error of the input clock affects the divided clock period of the TO00 output.

The period of the TO00 output clock includes a sampling error of one period of the operation clock.

Clock period of TO00 output = Ideal TO00 output clock period ± Operation clock period (error)

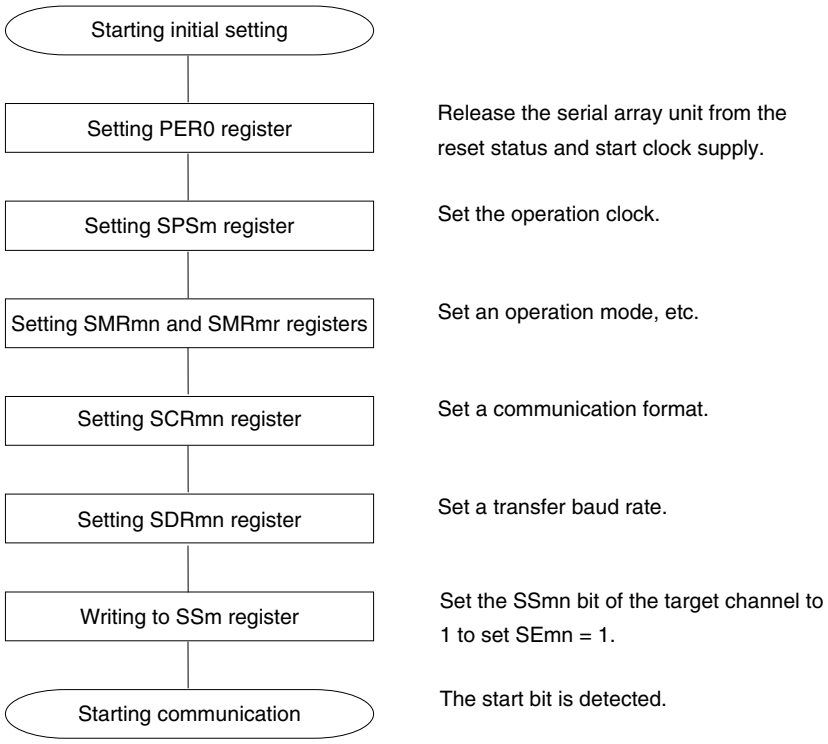
TDR00 can be rewritten at any time. The new value of TDR00 becomes valid during the next count period.

Figure 7-43. Block Diagram of Operation as Frequency Divider



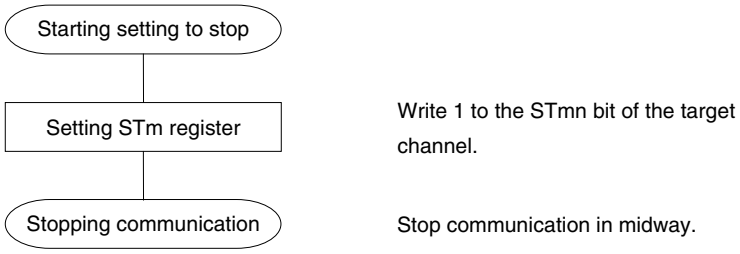
(2) Operation procedure

Figure 13-80. Initial Setting Procedure for UART Reception

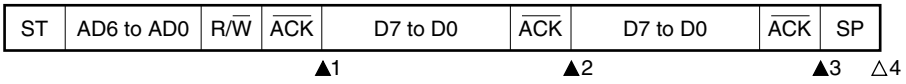


Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Figure 13-81. Procedure for Stopping UART Reception



(ii) When WTIM0 = 1

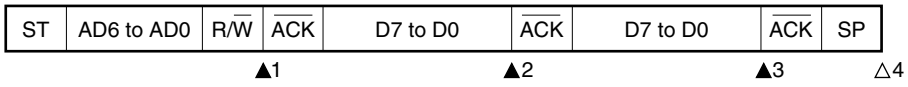


▲1: IICS0 = 0101×110B
▲2: IICS0 = 0001×100B
▲3: IICS0 = 0001××00B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(b) When arbitration loss occurs during transmission of extension code

(i) When WTIM0 = 0



▲1: IICS0 = 0110×010B
▲2: IICS0 = 0010×000B
▲3: IICS0 = 0010×000B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

17.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 17-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 17-10 shows multiple interrupt servicing examples.

Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	×	○	×	○	×	○	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP0, ISP1, and IE are flags contained in the PSW.

ISP1 = 0, ISP0 = 0: An interrupt of level 1 or level 0 is being serviced.

ISP1 = 0, ISP0 = 1: An interrupt of level 2 is being serviced.

ISP1 = 1, ISP0 = 0: An interrupt of level 3 is being serviced.

ISP1 = 1, ISP0 = 1: Wait for An interrupt acknowledgment.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

4. PR is a flag contained in PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)

PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1

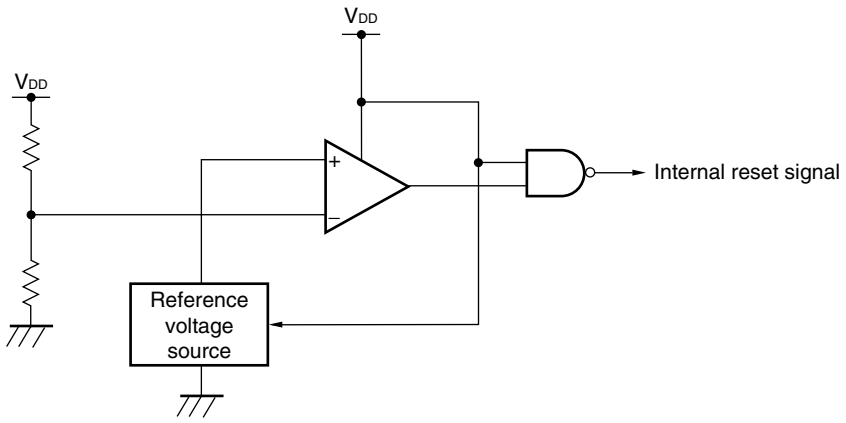
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0

PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)

21.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 21-1.

Figure 21-1. Block Diagram of Power-on-Clear Circuit



21.3 Operation of Power-on-Clear Circuit

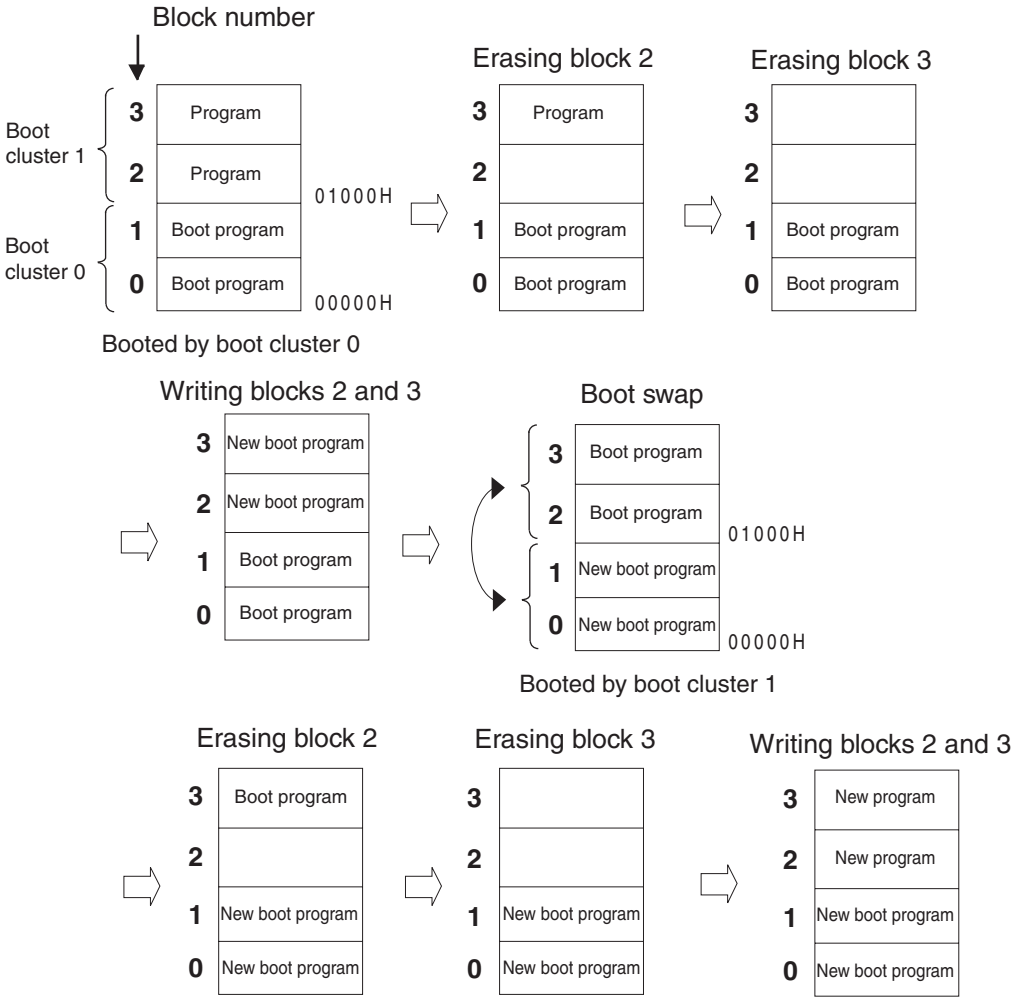
- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{POC} = 1.59 V ±0.09 V), the reset status is released.

  Caution If the low-voltage detector (LVI) is set to ON by an option byte by default, the reset signal is not released until the supply voltage (V_{DD}) exceeds 2.07 V ±0.2 V.

- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.09 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

Figure 25-13. Example of Executing Boot Swapping



<R> **(4) X1 oscillation: Crystal resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)**

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Co., Ltd.	HC49SFWB16000D0PPTZZ	Lead	16.0	10	10	1.8	5.5
	CX49GFWB16000D0PPTZZ						
	CX1255GB16000D0PPTZZ	SMD					
	CX8045GB16000D0PPTZZ						
	CX5032GB16000D0PPTZZ						
	CX5032SB16000D0PPTZZ						
	CX3225GB16000D0PPTZZ						
	CX3225SB16000D0PPTZZ						
	CX2520SB16000D0PPTZZ						
	HC49SFWB20000D0PPTZZ	Lead	20.0	10	10	2.3	
	CX49GFWB20000D0PPTZZ						
	CX1255GB20000D0PPTZZ	SMD					
	CX8045GB20000D0PPTZZ						
	CX5032GB20000D0PPTZZ						
	CX5032SB20000D0PPTZZ						
	CX3225GB20000D0PPTZZ						
	CX3225SB20000D0PPTZZ						
	CX2520SB20000D0PPTZZ						
	CX2016SB20000D0PPTZZ						

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KG3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

<R> **(2) X1 oscillation: Crystal resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)**

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Co., Ltd.	HC49SFWB04194D0PPTZZ	Lead	4.194	10	10	1.8	5.5
	CX49GFWB04194D0PPTZZ						
	CX1255GB04194D0PPTZZ	SMD					
	HC49SFWB05000D0PPTZZ	Lead	5.0	10	10	1.8	
	CX49GFWB05000D0PPTZZ						
	CX1255GB05000D0PPTZZ	SMD					
	CX8045GB05000D0PPTZZ						
	HC49SFWB08380D0PPTZZ	Lead	8.38	10	10	1.8	
	CX49GFWB08380D0PPTZZ						
	CX1255GB08380D0PPTZZ	SMD					
	CX8045GB08380D0PPTZZ						
	CX5032GB08380D0PPTZZ						
	HC49SFWB10000D0PPTZZ	Lead	10.0	10	10	1.8	
	CX49GFWB10000D0PPTZZ						
	CX1255GB10000D0PPTZZ	SMD					
	CX8045GB10000D0PPTZZ						
	CX5032GB10000D0PPTZZ						
	CX5032SB10000D0PPTZZ						
	CX3225GB10000D0PPTZZ						

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KG3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (13/16)

μPD78F1167A(A), 78F1168A(A)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +70°C	V_{DD} = 5.0 V		6.4	36.0	μA
				V_{DD} = 3.0 V		6.4	36.0	μA
				V_{DD} = 2.0 V		6.3	32.8	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +85°C	V_{DD} = 5.0 V		6.4	51.0	μA
				V_{DD} = 3.0 V		6.4	51.0	μA
				V_{DD} = 2.0 V		6.3	47.8	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF0}, and AV_{REF1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When internal high-speed oscillator and high-speed system clock are stopped. When watchdog timer is stopped.

Remarks 1. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

<R> **2.** Temperature condition of the TYP. value is T_A = 25°C

(3) Serial interface: Serial array unit (12/18)

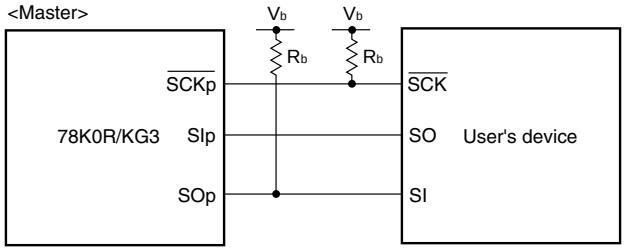
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

<R> **(f) During communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to $\overline{SCKp}$↓)[Note]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	100			ns
SIp hold time (from $\overline{SCKp}$↓)[Note]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↑ to SOp output[Note]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			40	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			40	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for SIp and the N-ch open-drain output (V_{DD} tolerance) mode for SOp and $\overline{SCKp}$ by using the PIMg and POMg registers.

Remarks 1. p: CSI number (p = 01, 10, 20), g: PIM and POM number (g = 0, 4, 14)

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

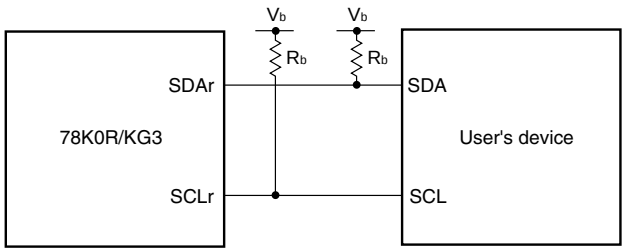
3. R_b[Ω]: Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

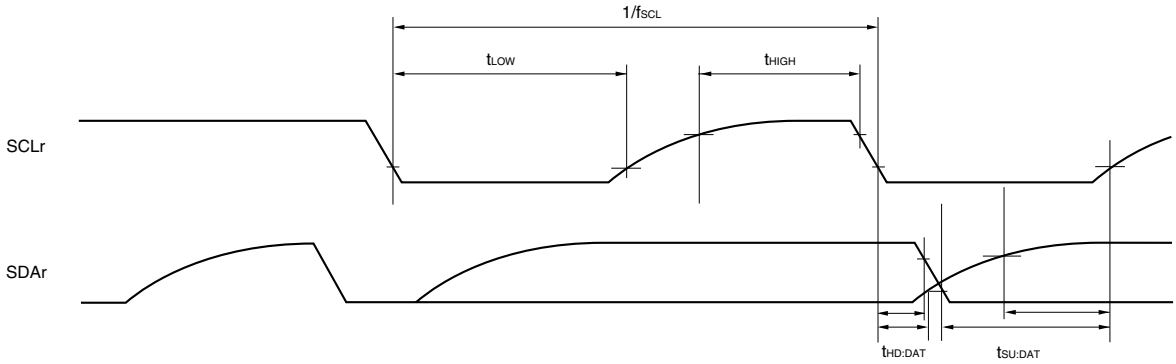
5. CSI00 cannot communicate at different potential. Use CSI01, CSI10, and CSI20 for communication at different potential.

(3) Serial interface: Serial array unit (18/18)

Simplified I^2C mode connection diagram (during communication at different potential)



Simplified I^2C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDAr and the N-ch open-drain output (V_{DD} tolerance) mode for SCLr by using the PIMg and POMg registers.

Remarks 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $V_b[V]$: Communication line voltage

2. r: IIC number (r = 10, 20), g: PIM and POM number (g = 0, 14)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 17	Soft	Interrupt functions	PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H: Priority specification flag registers	Be sure to set bits 1 to 7 of PR02H and PR12H to 1.	p.644 □
			EGP0, EGP1: External interrupt rising edge enable registers, EGN0, EGN1: External interrupt falling edge enable registers	Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.	p.646 □
			Software interrupt request acknowledgment	Do not use the RETI instruction for restoring from the software interrupt.	p.650 □
			BRK instruction	The BRK instruction is not one of the above-listed interrupt request hold instructions. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged.	p.654 □
Chapter 18	Soft	Key interrupt function	KRM: Key return mode register	If any of the KRM0 to KRM7 bits used is set to 1, set bits 0 to 7 (PU70 to PU77) of the corresponding pull-up resistor register 7 (PU7) to 1.	p.656 □
				An interrupt will be generated if the target bit of the KRM register is set while a low level is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling interrupt servicing by using the interrupt mask flag. Afterward, clear the interrupt request flag and enable interrupt servicing after waiting for the key interrupt input low-level width (250 ns or more).	p.656 □
				The bits not used in the key interrupt mode can be used as normal ports.	p.656 □
Chapter 19	Soft	Standby function	–	The STOP mode can be used only when the CPU is operating on the main system clock. The STOP mode cannot be set while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.	p.657 □
				When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.	p.657 □
				The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.	p.657 □

(4/5)

Page	Description	Classification
CHAPTER 16 DMA CONTROLLER (continuation)		
p.627	Addition of **Note** to **Figure 16-12. Example of Setting for Holding DMA Transfer Pending by DWAITn**	(c)
pp.628, 629	Change of **16.5.7 Forced termination by software**	(c)
p.630	Change of **(1) Priority of DMA** in **16.6 Cautions on Using DMA Controller**	(c)
p.631	Change of **(2) DMA response time** in **16.6 Cautions on Using DMA Controller**	(c)
p.632	Change of description in **(4) DMA pending instruction** in **16.6 Cautions on Using DMA Controller**	(c)
CHAPTER 17 INTERRUPT FUNCTIONS		
p.636	Change of **(B) External maskable interrupt (INTPn)** in **Figure 17-1. Basic Configuration of Interrupt Function**	(c)
p.637	Addition of **(C) External maskable interrupt (INTKR)** to **Figure 17-1. Basic Configuration of Interrupt Function**	(c)
p.654	Addition of **instruction** to **17.4.4 Interrupt request hold**	(c)
CHAPTER 18 KEY INTERRUPT FUNCTION		
p.655	Change of **Table 18-2. Configuration of Key Interrupt**	(c)
p.656	Addition of **18.3 (2) Port mode register 7 (PM7)**	(c)
CHAPTER 27 BCD CORRECTION CIRCUIT		
p.740	Change of **27.3 BCD Correction Circuit Operation**	(a)
CHAPTER 28 INSTRUCTION SET		
p.745	Change of description in **28.1.4 PREFIX instruction**	(c)
p.761	Change of **Clocks** of **BT Mnemonic** in **Table 28-5. Operation List (16/17)**	(c)
p.762	Change of **Clocks** of **BF Mnemonic** in **Table 28-5. Operation List (17/17)**	(c)
CHAPTER 29 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)		
p.765	Deletion of **Remark** in **X1 Oscillator Characteristics**	(a)
p.767	Deletion of **Remark** in **XT1 Oscillator Characteristics**	(a)
pp.768, 770, 772	Change of **Caution** in **Recommended Oscillator Constants**	(c)
pp.769, 771	Addition of KYOCERA KINSEKI Co., Ltd. to **Recommended Oscillator Constants**	(c)
pp.780 to 788	Addition of **Remark** to Supply current in **DC Characteristics**	(c)
p.801	Change of **(b) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCK}}$p... internal clock output)** in **Serial interface: Serial array unit**	(b)
p.802	Change of **(c) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCK}}$p... external clock input)** in **Serial interface: Serial array unit**	(b)
p.804	Addition of **Note** to **(d) During communication at same potential (simplified I^2C mode)** in **Serial interface: Serial array unit**	(c)
pp.810, 811	Change of **(f) During communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{\text{SCK}}$p... internal clock output)** in **Serial interface: Serial array unit**	(b)
p.813	Change of **(g) During communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{\text{SCK}}$p... external clock input)** in **Serial interface: Serial array unit**	(b)
p.816	Addition of **Note** to **(h) During communication at different potential (2.5 V, 3 V) (simplified I^2C mode)** in **Serial interface: Serial array unit**	(b)

Remark "Classification" in the above table classifies revisions as follows.

(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents